Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	76	("plurality request" or request$2) and recall and ("data objects" or "data object") and migration and queue$2 and @ad<"20010215"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 09:25
L2	50	("plurality request" or request$2) same queue$ and recall and ("data objects" or "data object") and migration and queue$2 and @ad<"20010215"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 08:27
L3	108	"first queue" and recall$3 and queue$1 and @ad<"20010215"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 08:43
L4	2	2 and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 08:33
L5	27	("plurality request" or request$2) and offset$1 same monotonical$4 same increas$4 and sequence$2 and @ad<"20010215"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 08:41
L6	11	5 and timestamp$1 and queue$1	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 08:42
L7	1	3 and (timestamp$1 same queue$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 08:43
L8	200	("plurality request" or request$2) and (queues same timestamp$1) and @ad<"20010215"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 09:26
L9	67	("plurality request" or request$2) same (queues same timestamp$1) and @ad<"20010215"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 09:32
L10	2	("plurality request" or request$2) same ((creat$3 near2 queues) same timestamp$1) and @ad<"20010215"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 09:27
L11	12	("plurality request" or request$2) same (creat$3 same queues same timestamp$1) and @ad<"20010215"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 09:36

L12	54	timestamp$1 near2 queue$1 and @ad<"20010215"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 09:36
L13	0	("plurality request" or request$2) adj recall same ("data objects" or "data object") same migration same queue$2 and @ad<"20010215"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 10:02
L14	1	(migration and "first queue" and @ad<"20010215") and (migration near10 recall and @ad<"20010215" and ("data objects" or "data object") and ("plurality request" or request$2) and queue$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 10:02
L15	3	VOB and migration and @ad<"20010215"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 10:03
L16	0	pluralit$3 same media same writeable and concurrency and @ad<"0010215"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 10:03
L17	9	(Plurality near5 media) adj10 writeable	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 10:04
L18	0	17 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 10:04
L19	0	9 and 17	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 10:05
L20	0	8 and 17	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/02/28 10:05

PORTAL
US Patent & Trademark Office

Subscribe (Full Service) Register (Limited Service, Free) Login

Search: The ACM Digital Library The Guide

first queue and recall request

THE ACM DIGITAL LIBRARY

Feedback Report a problem Satisfaction survey

Terms used **first queue** and **recall request** Found **52,871** of **150,885**

Sort results by: relevance
Display results: expanded form
Save results to a Binder
Search Tips
Open results in a new window

Try an Advanced Search
Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next
Best 200 shown Relevance scale

1 The architecture of a Linda coprocessor
V. Krishnaswamy, S. Ahuja, N. Carriero, D. Gelernter
May 1988 **ACM SIGARCH Computer Architecture News , Proceedings of the 15th Annual International Symposium on Computer architecture**, Volume 16 Issue 2
Full text available: pdf(1.09 MB) Additional Information: full citation, abstract, references, citings, index terms

We describe the architecture of a coprocessor that supports the communication primitives of the Linda parallel programming environment in hardware. The coprocessor is a critical element in the architecture of the Linda Machine, an MIMD parallel processing system that is designed top down from the specifications of Linda. Communication in Linda programs takes place through a logically shared associative memory mechanism called tuple space. The Linda Machine, however, has no physically shared ...

2 Semantic lock models in object-oriented distributed systems and deadlock resolution
M. Roesler, W. A. Burkhard
June 1988 **ACM SIGMOD Record , Proceedings of the 1988 ACM SIGMOD international conference on Management of data**, Volume 17 Issue 3
Full text available: pdf(1.14 MB) Additional Information: full citation, abstract, references, citings, index terms

We propose a distributed algorithm for detection and resolution of resource deadlocks in object-oriented distributed systems. The algorithm proposed is shown to detect and resolve all O(n1) cycles present in the worst case waits-for-graph (WFG) with n vertices by transmitting O(n3) messages of small constant size. Its average time complexity has been shown to be O(ne), where e is the number of edges in the WFG After deadlock resolution, the ...

3 Fishspear: a priority queue algorithm
Michael J. Fischer, Michael S. Paterson
January 1994 **Journal of the ACM (JACM)**, Volume 41 Issue 1
Full text available: pdf(1.73 MB) Additional Information: full citation, abstract, references, citings, index terms, review

The Fishspear priority queue algorithm is presented and analyzed. Fishspear is comparable to the usual heap algorithm in its worst-case running time, and its relative performance is much better in many common situations. Fishspear also differs from the heap method in that it can be implemented efficiently using sequential storage such as stacks or tapes, making it potentially attractive for implementation of very large queues on paged memory

systems.

Keywords: comparison count, complexity analysis, heap, online algorithm, priority queue, running time, sequential storage

4 Interposed proportional sharing for a storage service utility

Wei Jin, Jeffrey S. Chase, Jasleen Kaur

June 2004 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the joint international conference on Measurement and modeling of computer systems**, Volume 32 Issue 1

Full text available: pdf(339.02 KB) Additional Information: full citation, abstract, references, index terms

This paper develops and evaluates new share-based scheduling algorithms for differentiated service quality in network services, such as network storage servers. This form of resource control makes it possible to share a server among multiple request flows with probabilistic assurance that each flow receives a specified minimum share of a server's capacity to serve requests. This assurance is important for safe outsourcing of services to shared utilities such as Storage Service Providers.Our appr ...

Keywords: differentiated service, fair sharing, multiprocessor scheduling, performance isolation, proportional sharing, quality of service, storage services, utility computing, weighted fair queuing

5 A systems programming course using the HMS 5050, a counterfeit, hands-on, large-scale computer system

Bernhard Weinberg, Leonard H. Weiner

January 1974 **ACM SIGCSE Bulletin , Proceedings of the fourth SIGCSE technical symposium on Computer science education**, Volume 6 Issue 1

Full text available: pdf(647.07 KB) Additional Information: full citation, abstract, references, citings, index terms

Computer Science students at MSU design and implement multiprogramming monitors for a simulated computer system which is an amalgamation of Control Data 3000- and 6000-series machines. In this paper we describe this computer, the systems programming course in which it is used, and the students' project. We also report briefly on student performance.

6 A unified wireless LAN architecture for real-time and non-real-time communication services

Sunghyun Choi, Kang G. Shin

February 2000 **IEEE/ACM Transactions on Networking (TON)**, Volume 8 Issue 1

Full text available: pdf(298.12 KB) Additional Information: full citation, references, citings, index terms, review

Keywords: MAC protocol, QoS-sensitive communication, admission tests, dynamic time-division duplexing (D-TDD), location-dependent errors, polling, priority scheduling, wireless LAN

7 Design and performance evaluation of an RRA scheme for voice-data channel access in outdoor microcellular environments

Allan C. Cleary, Michael Paterakis

June 1997 **Mobile Networks and Applications**, Volume 2 Issue 1

Full text available: pdf(398.19 KB) Additional Information: full citation, abstract, references, citings, index terms

In PCS networks, the multiple access problem is characterized by spatially dispersed mobile source terminals sharing a radio channel connected to a fixed base station. In this paper, we design and evaluate a reservation random access (RRA) scheme that multiplexes voice traffic at the talkspurt level to efficiently integrate voice and data traffic in outdoor microcellular environments. The scheme involves partitioning the time frame into two request intervals (voice and data) and an informat ...

8 Ensuring robust call throughput and fairness for SCP overload controls

Donald E. Smith

October 1995 **IEEE/ACM Transactions on Networking (TON)**, Volume 3 Issue 5

Full text available: pdf(1.21 MB) Additional Information: full citation, references, citings, index terms

9 Using a user-level memory thread for correlation prefetching

Yan Solihin, Jaejin Lee, Josep Torrellas

May 2002 **ACM SIGARCH Computer Architecture News**, Volume 30 Issue 2

Full text available: pdf(1.46 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper introduces the idea of using a User-Level Memory Thread (ULMT) for correlation prefetching. In this approach, a user thread runs on a general-purpose processor in main memory, either in the memory controller chip or in a DRAM chip. The thread performs correlation prefetching in software, sending the prefetched data into the L2 cache of the main processor. This approach requires minimal hardware beyond the memory processor: the correlation table is a software data structure that reside ...

Keywords: data prefetching, intelligent memory, processing-in-memory, computer architecture, correlation prefetching, memory hierarchies, caches, threads

10 A General Model for the Performance of Disk Systems

Neil C. Wilhelm

January 1977 **Journal of the ACM (JACM)**, Volume 24 Issue 1

Full text available: pdf(911.47 KB) Additional Information: full citation, abstract, references, citings, index terms

The performance of a disk system is often measured in terms of the length of the waiting line or queue of requests for each of the system's spindles. Thus it is natural to formulate and analyze queueing models of disk systems. While most disk systems have certain characteristics, such as channel interference and concurrent seeks, in common, previous analyses have always been begun from scratch, without exploiting this commonality. We introduce a general queueing model for disk systems, whic ...

11 Locking performance in centralized databases

Y. C. Tay, Nathan Goodman, R. Suri

December 1985 **ACM Transactions on Database Systems (TODS)**, Volume 10 Issue 4

Full text available: pdf(3.25 MB) Additional Information: full citation, abstract, references, citings, index terms

An analytic model is used to study the performance of dynamic locking. The analysis uses only the steady-state average values of the variables. The solution to the model is given by a cubic, which has exactly one valid root for the range of parametric values that is of

interest. The model's predictions agree well with simulation results for transactions that require up to twenty locks. The model separates data contention from resource contention, thus facilitating an analysis of their separ ...

12 Performance of a mirrored disk in a real-time transaction system
Shenze Chen, Don Towsley
April 1991 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1991 ACM SIGMETRICS conference on Measurement and modeling of computer systems**, Volume 19 Issue 1
Full text available: pdf(975.06 KB) Additional Information: full citation, references, index terms

13 Virtual clock: a new traffic control algorithm for packet switching networks
L. Zhang
August 1990 **ACM SIGCOMM Computer Communication Review , Proceedings of the ACM symposium on Communications architectures & protocols**, Volume 20 Issue 4
Full text available: pdf(1.19 MB) Additional Information: full citation, abstract, references, citings, index terms

A challenging research issue in high speed networking is how to control the transmission rate of statistical data flows. This paper describes a new algorithm, VirtualClock, for data traffic control in high-speed networks. VirtualClock maintains the statistical multiplexing flexibility of pocket switching while ensuring each data flow its reserved average throughput rate at the same time. The algorithm has been tested through simulation.

14 A measurement-based admission control algorithm for integrated services packet networks
Sugih Jamin, Peter B. Danzig, Scott Shenker, Lixia Zhang
October 1995 **ACM SIGCOMM Computer Communication Review , Proceedings of the conference on Applications, technologies, architectures, and protocols for computer communication**, Volume 25 Issue 4
Full text available: pdf(1.67 MB) Additional Information: full citation, abstract, references, citings, index terms

Many designs for integrated service networks offer a bounded delay packet delivery service to support real-time applications. To provide bounded delay service, networks must use admission control to regulate their load. Previous work on admission control mainly focused on algorithms that compute the worst case theoretical queueing delay to guarantee an absolute delay bound for all packets. In this paper we describe a *measurement-based* admission control algorithm for *predictive* serv ...

15 A priority scheme for the IEEE 802.14 MAC protocol for hybrid fiber-coax networks
Mark D. Corner, Jörg Liebeherr, Nada Golmie, Chatschik Bisdikian, David H. Su
April 2000 **IEEE/ACM Transactions on Networking (TON)**, Volume 8 Issue 2
Full text available: pdf(300.06 KB) Additional Information: full citation, references, citings, index terms

Keywords: local area networks, quality-of-service

16 Coordinating heterogeneous time-based media between independent applications
Scott Flinn
January 1995 **Proceedings of the third ACM international conference on Multimedia**

Full text available: html(53.68 KB) Additional Information: full citation, references, index terms

Keywords: auditory display, distributed systems, media integration and synchronization, operating system support, real-time scheduling, system architecture

17 Informed prefetching of collective input/output requests
Tara M. Madhyastha, Garth A. Gibson, Christos Faloutsos
January 1999 **Proceedings of the 1999 ACM/IEEE conference on Supercomputing (CDROM)**
Full text available: pdf(163.14 KB) Additional Information: full citation, references, index terms

18 Using feedback to control tree saturation in multistage interconnection networks
S. L. Scott, G. S. Sohi
April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the 16th annual international symposium on Computer architecture**, Volume 17 Issue 3
Full text available: pdf(1.10 MB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we propose the use of feedback schemes in multiprocessors which use an interconnection network with distributed routing control. We show that by altering system behavior so as to minimize the occurrence of a performance-degrading situation in the network, the overall throughout of the system can be improved. As an example, we have considered the problem of tree saturation caused by hot spots in multistage interconnection networks. Tree saturation degrades the perfo ...

19 Memory coherence in shared virtual memory systems
Kai Li, Paul Hudak
November 1989 **ACM Transactions on Computer Systems (TOCS)**, Volume 7 Issue 4
Full text available: pdf(2.71 MB) Additional Information: full citation, abstract, references, citings, index terms, review

The memory coherence problem in designing and implementing a shared virtual memory on loosely coupled multiprocessors is studied in depth. Two classes of algorithms, centralized and distributed, for solving the problem are presented. A prototype shared virtual memory on an Apollo ring based on these algorithms has been implemented. Both theoretical and practical results show that the memory coherence problem can indeed be solved efficiently on a loosely coupled multiprocessor.

20 Graphic time-sharing with real-time data bases
Jesse B. Hillman
August 1969 **Proceedings of the 1969 24th national conference**
Full text available: pdf(770.17 KB) Additional Information: full citation, abstract, index terms

This system is being developed to process flight test data for the McDonnell-Douglas Corporation to significantly reduce flight test development and certification time and to reduce data processing costs. It is a time-sharing system using graphic cathode ray tube terminals. The system consists of nine processors: a Sigma 7 central processing unit, three general-purpose input/output processors, two special telemetry decommutator channels and three Sigma 2 central processor units.< ...

The ACM Portal is published by the Association for Computing Machinery. Copyright © 2005 ACM, Inc.
Terms of Usage Privacy Policy Code of Ethics Contact Us

Useful downloads: Adobe Acrobat QuickTime Windows Media Player Real Player

PORTAL
US Patent & Trademark Office

Subscribe (Full Service) Register (Limited Service, Free) Login

Search: The ACM Digital Library The Guide

plurality request and recall and data objects and migration and

THE ACM DIGITAL LIBRARY

Feedback Report a problem Satisfaction survey

Terms used
plurality request and **recall** and **data objects** and **migration** and **queues**

Found **44,227** of **150,885**

Sort results by: relevance
Display results: expanded form
Save results to a Binder
Search Tips
Open results in a new window

Try an Advanced Search
Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next
Best 200 shown Relevance scale

1 Fast detection of communication patterns in distributed executions
Thomas Kunz, Michiel F. H. Seuren
November 1997 **Proceedings of the 1997 conference of the Centre for Advanced Studies on Collaborative research**
Full text available: pdf(4.21 MB) Additional Information: full citation, abstract, references, index terms

Understanding distributed applications is a tedious and difficult task. Visualizations based on process-time diagrams are often used to obtain a better understanding of the execution of the application. The visualization tool we use is Poet, an event tracer developed at the University of Waterloo. However, these diagrams are often very complex and do not provide the user with the desired overview of the application. In our experience, such tools display repeated occurrences of non-trivial commun ...

2 "Topologies"—distributed objects on multicomputers
Karsten Schwan, Win Bo
May 1990 **ACM Transactions on Computer Systems (TOCS)**, Volume 8 Issue 2
Full text available: pdf(3.83 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Application programs written for large-scale multicomputers with interconnection structures known to the programmer (e.g., hypercubes or meshes) use complex communication structures for connecting the applications' parallel tasks. Such structures implement a wide variety of functions, including the exchange of data or control information relevant to the task computations and/or the communications required for task synchronization, message forwarding/filtering under program control, and so o ...

3 Data partitioning and load balancing in parallel disk systems
Peter Scheuermann, Gerhard Weikum, Peter Zabback
February 1998 **The VLDB Journal — The International Journal on Very Large Data Bases**, Volume 7 Issue 1
Full text available: pdf(310.27 KB) Additional Information: full citation, abstract, index terms

Parallel disk systems provide opportunities for exploiting I/O parallelism in two possible ways, namely via inter-request and intra-request parallelism. In this paper, we discuss the main issues in performance tuning of such systems, namely striping and load balancing, and show their relationship to response time and throughput. We outline the main components of an intelligent, self-reliant file system that aims to optimize striping by taking into account the requirements of the applications, an ...

Keywords: Data allocation, Disk cooling, File striping, Load balancing, Parallel disk systems, Performance tuning

4 Concurrency and distribution in object-oriented programming

Jean-Pierre Briot, Rachid Guerraoui, Klaus-Peter Lohr

September 1998 **ACM Computing Surveys (CSUR)**, Volume 30 Issue 3

Full text available: pdf(289.34 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper aims at discussing and classifying the various ways in which the object paradigm is used in concurrent and distributed contexts. We distinguish among the library approach, the integrative approach, and the reflective approach. The library approach applies object-oriented concepts, as they are, to structure concurrent and distributed systems through class libraries. The integrative approach consists of merging concepts such as obj ...

Keywords: concurrency, distribution, integration, libraries, message passing, object, reflection

5 Distributed file systems: concepts and examples

Eliezer Levy, Abraham Silberschatz

December 1990 **ACM Computing Surveys (CSUR)**, Volume 22 Issue 4

Full text available: pdf(5.33 MB) Additional Information: full citation, abstract, references, citings, index terms, review

The purpose of a distributed file system (DFS) is to allow users of physically distributed computers to share data and storage resources by using a common file system. A typical configuration for a DFS is a collection of workstations and mainframes connected by a local area network (LAN). A DFS is implemented as part of the operating system of each of the connected computers. This paper establishes a viewpoint that emphasizes the dispersed structure and decentralization of both data and con ...

6 Rover: a toolkit for mobile information access

A. D. Joseph, A. F. de Lespinasse, J. A. Tauber, D. K. Gifford, M. F. Kaashoek

December 1995 **ACM SIGOPS Operating Systems Review , Proceedings of the fifteenth ACM symposium on Operating systems principles**, Volume 29 Issue 5

Full text available: pdf(2.18 MB) Additional Information: full citation, references, citings, index terms

7 Integrated document caching and prefetching in storage hierarchies based on Markov-chain predictions

Achim Kraiss, Gerhard Weikum

August 1998 **The VLDB Journal — The International Journal on Very Large Data Bases**, Volume 7 Issue 3

Full text available: pdf(603.01 KB) Additional Information: full citation, abstract, citings, index terms

Large multimedia document archives may hold a major fraction of their data in tertiary storage libraries for cost reasons. This paper develops an integrated approach to the vertical data migration between the tertiary, secondary, and primary storage in that it reconciles speculative prefetching, to mask the high latency of the tertiary storage, with the replacement policy of the document caches at the secondary and primary storage level, and also considers the interaction of these policies with ...

Keywords: Caching, Markov chains, Performance, Prefetching, Scheduling, Stochastic

modeling, Tertiary storage

8 Communication optimizations for parallel computing using data access information
Martin C. Rinard
December 1995 **Proceedings of the 1995 ACM/IEEE conference on Supercomputing (CDROM)**
Full text available: html(67.34 KB) Additional Information: full citation, references, citings, index terms

9 A shared, segmented memory system for an object-oriented database
Mark F. Hornick, Stanley B. Zdonik
January 1987 **ACM Transactions on Information Systems (TOIS)**, Volume 5 Issue 1
Full text available: pdf(2.05 MB) Additional Information: full citation, abstract, references, citings, index terms, review

This paper describes the basic data model of an object-oriented database and the basic architecture of the system implementing it. In particular, a secondary storage segmentation scheme and a transaction-processing scheme are discussed. The segmentation scheme allows for arbitrary clustering of objects, including duplicates. The transaction scheme allows for many different sharing protocols ranging from those that enforce serializability to those that are nonserializable and require communi ...

10 Migrating sockets—end system support for networking with quality of service guarantees
David K. Y. Yau, Simon S. Lam
December 1998 **IEEE/ACM Transactions on Networking (TON)**, Volume 6 Issue 6
Full text available: pdf(369.10 KB) Additional Information: full citation, references, index terms

Keywords: CPU scheduling, bandwidth scheduling, packet demultiplexing, quality of service guarantees, user level protocol

11 Computer Communication Networks: Approaches, Objectives, and Performance Considerations
Stephen R. Kimbleton, G. Michael Schneider
September 1975 **ACM Computing Surveys (CSUR)**, Volume 7 Issue 3
Full text available: pdf(3.99 MB) Additional Information: full citation, references, citings, index terms

12 Data locality and load balancing in COOL
Rohit Chandra, Anoop Gupta, John L. Hennessy
July 1993 **ACM SIGPLAN Notices , Proceedings of the fourth ACM SIGPLAN symposium on Principles and practice of parallel programming**, Volume 28 Issue 7
Full text available: pdf(1.36 MB) Additional Information: full citation, abstract, references, citings, index terms

Large-scale shared memory multiprocessors typically support a multilevel memory hierarchy consisting of per-processor caches, a local portion of shared memory, and remote shared memory. On such machines, the performance of parallel programs is often limited by the high latency of remote memory references. In this paper we explore how knowledge of the underlying memory hierarchy can be used to schedule computation and distribute data

structures, and thereby improve data locality. Our study i ...

13 Input/Output: Energy conservation techniques for disk array-based servers



Eduardo Pinheiro, Ricardo Bianchini

June 2004 **Proceedings of the 18th annual international conference on Supercomputing**

Full text available: pdf(174.29 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we study energy conservation techniques for disk array-based network servers. First, we introduce a new conservation technique, called Popular Data Concentration (PDC), that migrates frequently accessed data to a subset of the disks. The goal is to skew the load towards a few of the disks, so that others can be transitioned to low-power modes. Next, we introduce a user-level file server that takes advantage of PDC. In the context of this server, we compare PDC to the Massive Array ...

Keywords: disk power, energy conservation, network servers

14 Supporting dynamic data structures on distributed-memory machines



Anne Rogers, Martin C. Carlisle, John H. Reppy, Laurie J. Hendren

March 1995 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 17 Issue 2

Full text available: pdf(2.05 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Compiling for distributed-memory machines has been a very active research area in recent years. Much of this work has concentrated on programs that use arrays as their primary data structures. To date, little work has been done to address the problem of supporting programs that use pointer-based dynamic data structures. The techniques developed for supporting SPMD execution of array-based programs rely on the fact that arrays are statically defined and directly addressable. Recursive data s ...

Keywords: dynamic data structures

15 The design, implementation, and evaluation of Jade



Martin C. Rinard, Monica S. Lam

May 1998 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 20 Issue 3

Full text available: pdf(575.88 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Jade is a portable, implicitly parallel language designed for exploiting task-level concurrency.Jade programmers start with a program written in a standard serial, imperative language, then use Jade constructs to declare how parts of the program access data. The Jade implementation uses this data access information to automatically extract the concurrency and map the application onto the machine at hand. The resulting parallel execution preserves the semantics of the original serial program ...

Keywords: parallel computing, parallel programming languages

16 Recovery protocols for shared memory database systems



Lory D. Molesky, Krithi Ramamritham

May 1995 **ACM SIGMOD Record , Proceedings of the 1995 ACM SIGMOD international conference on Management of data**, Volume 24 Issue 2

Full text available: pdf(1.65 MB) Additional Information: full citation, abstract, references, index terms

Significant performance advantages can be gained by implementing a database system on a cache-coherent shared memory multiprocessor. However, problems arise when failures occur. A single node (where a *node* refers to a processor/memory pair) crash may require a reboot of the entire shared memory system. Fortunately, shared memory multiprocessors that isolate individual node failures are currently being developed. Even with these, because of the side effects of the cache coherency protocol, ...

17 Reliable communication in the presence of failures

Kenneth P. Birman, Thomas A. Joseph

January 1987 **ACM Transactions on Computer Systems (TOCS)**, Volume 5 Issue 1

Full text available: pdf(2.62 MB) Additional Information: full citation, abstract, references, citings, index terms, review

The design and correctness of a communication facility for a distributed computer system are reported on. The facility provides support for fault-tolerant process groups in the form of a family of reliable multicast protocols that can be used in both local- and wide-area networks. These protocols attain high levels of concurrency, while respecting application-specific delivery ordering constraints, and have varying cost and performance that depend on the degree of ordering ...

18 Process mobility in distributed-memory simulation systems

Janche Sang, Edward Mascarenhas, Vernon Rego

December 1993 **Proceedings of the 25th conference on Winter simulation**

Full text available: pdf(817.32 KB) Additional Information: full citation, references, citings

19 Ordered shared locks for real-time databases

Divyakant Agrawal, Amr El Abbadi, Richard Jeffers, Lijing Lin

January 1995 **The VLDB Journal — The International Journal on Very Large Data Bases**, Volume 4 Issue 1

Full text available: pdf(2.11 MB) Additional Information: full citation, abstract, references

We propose locking protocols for real-time databases. Our approach has two main motivations: First, locking protocols are widely accepted and used in most database systems. Second, in real-time databases it has been shown that the blocking behavior of transactions in locking protocols results in performance degradation. We use a new relationship between locks called ordered sharing to eliminate blocking that arises in the traditional locking protocols. Ordered sharing eliminates blocking of read ...

Keywords: concurrency control, time-critical scheduling, transaction management

20 Reasoning about code mobility with mobile UNITY

Gian Pietro Picco, Gruia-Catalin Roman, Peter J. McCann

July 2001 **ACM Transactions on Software Engineering and Methodology (TOSEM)**, Volume 10 Issue 3

Full text available: pdf(419.80 KB) Additional Information: full citation, abstract, references, index terms

Advancements in network technology have led to the emergence of new computing paradigms that challenge established programming practices by employing weak forms of consistency and dynamic forms of binding. Code mobility, for instance, allows for invocation-time binding between a code fragment and the location where it executes. Similarly, mobile computing allows hosts (and the software they execute) to alter their physical location. Despite apparent similarities, the two paradigms are disti ...

Keywords: UNITY, code mobility, mobile agent

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

The ACM Portal is published by the Association for Computing Machinery. Copyright © 2005 ACM, Inc.
Terms of Usage Privacy Policy Code of Ethics Contact Us

Useful downloads: Adobe Acrobat QuickTime Windows Media Player Real Player

PORTAL
US Patent & Trademark Office

Subscribe (Full Service) Register (Limited Service, Free) Login

Search: The ACM Digital Library The Guide

plurality request and offsets and monotonically increasing and

THE ACM DIGITAL LIBRARY

Feedback Report a problem Satisfaction survey

Terms used
plurality request and **offsets** and **monotonically increasing** and **sequence**

Found **36,451** of **150,885**

Sort results by: relevance

Display results: expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Best 200 shown

Relevance scale

1 What TCP/IP protocol headers can tell us about the web

F. Donelson Smith, Félix Hernández Campos, Kevin Jeffay, David Ott

June 2001 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 2001 ACM SIGMETRICS international conference on Measurement and modeling of computer systems**, Volume 29 Issue 1

Full text available: pdf(1.55 MB) Additional Information: full citation, abstract, references, citings

We report the results of a large-scale empirical study of web traffic. Our study is based on over 500 GB of TCP/IP protocol-header traces collected in 1999 and 2000 (approximately one year apart) from the high-speed link connecting The University of North Carolina at Chapel Hill to its Internet service provider. We also use a set of smaller traces from the NLANR repository taken at approximately the same times for comparison. The principal results from this study are: (1) empirical data suitable ...

2 BASE: Using abstraction to improve fault tolerance

Miguel Castro, Rodrigo Rodrigues, Barbara Liskov

August 2003 **ACM Transactions on Computer Systems (TOCS)**, Volume 21 Issue 3

Full text available: pdf(436.18 KB) Additional Information: full citation, abstract, references, index terms

Software errors are a major cause of outages and they are increasingly exploited in malicious attacks. Byzantine fault tolerance allows replicated systems to mask some software errors but it is expensive to deploy. This paper describes a replication technique, BASE, which uses abstraction to reduce the cost of Byzantine fault tolerance and to improve its ability to mask software errors. BASE reduces cost because it enables reuse of off-the-shelf service implementations. It improves availability ...

Keywords: Byzantine fault tolerance, N-version programming, asynchronous systems, proactive recovery, state machine replication

3 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2

Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider

electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

4 Energy efficient indexing on air



Tomasz Imielinski, S. Viswanathan, B. R. Badrinath

May 1994 **ACM SIGMOD Record , Proceedings of the 1994 ACM SIGMOD international conference on Management of data**, Volume 23 Issue 2

Full text available: pdf(1.27 MB) Additional Information: full citation, abstract, references, citings, index terms

We consider wireless broadcasting of data as a way of disseminating information to a massive number of users. Organizing and accessing information on wireless communication channels is different from the problem of organizing and accessing data on the disk. We describe two methods, (1,m) Indexing and Distributed Indexing, for organizing and accessing broadcast data. We demonstrate that the proposed algorithms lead to significant improvement ...

5 Speeding up construction of PMR quadtree-based spatial indexes



Gisli R. Hjaltason, Hanan Samet

October 2002 **The VLDB Journal — The International Journal on Very Large Data Bases**, Volume 11 Issue 2

Full text available: pdf(355.72 KB) Additional Information: full citation, abstract, index terms

Spatial indexes, such as those based on the quadtree, are important in spatial databases for efficient execution of queries involving spatial constraints, especially when the queries involve spatial joins. In this paper we present a number of techniques for speeding up the construction of quadtree-based spatial indexes, specifically the PMR quadtree, which can index arbitrary spatial data. We assume a quadtree implementation using the "linear quadtree", a disk-resident representation ...

Keywords: Bulk-loading, I/O, Spatial indexing

6 RISCY patents



David A. Patterson

September 1988 **ACM SIGARCH Computer Architecture News**, Volume 16 Issue 4

Full text available: pdf(1.83 MB) Additional Information: full citation, index terms

7 Denial-of-service: A framework for classifying denial of service attacks



Alefiya Hussain, John Heidemann, Christos Papadopoulos

August 2003 **Proceedings of the 2003 conference on Applications, technologies, architectures, and protocols for computer communications**

Full text available: pdf(622.14 KB) Additional Information: full citation, abstract, references, citings, index terms

Launching a denial of service (DoS) attack is trivial, but detection and response is a painfully slow and often a manual process. Automatic classification of attacks as single- or multi-source can help focus a response, but current packet-header-based approaches are susceptible to spoofing. This paper introduces a framework for classifying DoS attacks based on header content, and novel techniques such as transient ramp-up behavior and spectral analysis. Although headers are easily forged, we sho ...

Keywords: denial of service attacks, measurement, security, time series analysis

8 Two-dimensional round-robin schedulers for packet switches with multiple input queues

Richard O. LaMaire, Dimitrios N. Serpanos

October 1994 **IEEE/ACM Transactions on Networking (TON)**, Volume 2 Issue 5

Full text available: pdf(1.24 MB) Additional Information: full citation, references, citings, index terms, review

9 Petal: distributed virtual disks

Edward K. Lee, Chandramohan A. Thekkath

September 1996 **Proceedings of the seventh international conference on Architectural support for programming languages and operating systems**, Volume 31 , 30 Issue 9 , 5

Full text available: pdf(1.19 MB) Additional Information: full citation, abstract, references, citings, index terms

The ideal storage system is globally accessible, always available, provides unlimited performance and capacity for a large number of clients, and requires no management. This paper describes the design, implementation, and performance of Petal, a system that attempts to approximate this ideal in practice through a novel combination of features. Petal consists of a collection of network-connected servers that cooperatively manage a pool of physical disks. To a Petal client, this collection appear ...

10 Location-aided routing (LAR) in mobile ad hoc networks

Young-Bae Ko, Nitin H. Vaidya

July 2000 **Wireless Networks**, Volume 6 Issue 4

Full text available: pdf(242.42 KB) Additional Information: full citation, references, citings, index terms

11 Anatomy of a native XML base management system

T. Fiebig, S. Helmer, C.-C. Kanne, G. Moerkotte, J. Neumann, R. Schiele, T. Westmann

December 2002 **The VLDB Journal — The International Journal on Very Large Data Bases**, Volume 11 Issue 4

Full text available: pdf(300.97 KB) Additional Information: full citation, abstract, index terms

Several alternatives to manage large XML document collections exist, ranging from file systems over relational or other database systems to specifically tailored XML base management systems. In this paper we give a tour of Natix, a database management system designed from scratch for storing and processing XML data. Contrary to the common belief that management of XML data is just another application for traditional databases like relational systems, we illustrate how almost every component in a ...

Keywords: Database, XML

12 Programming languages: Garbage collection for embedded systems

David F. Bacon, Perry Cheng, David Grove

September 2004 **Proceedings of the fourth ACM international conference on Embedded software**

Full text available: pdf(199.59 KB) Additional Information: full citation, abstract, references, index terms

Security concerns on embedded devices like cellular phones make Java an extremely

attractive technology for providing third-party and user-downloadable functionality. However, garbage collectors have typically required several times the maximum live data set size (which is the minimum possible heap size) in order to run well. In addition, the size of the virtual machine (ROM) image and the size of the collector's data structures (metadata) have not been a concern for server- or workstation-orien ...

Keywords: compaction, fragmentation, mark-and-sweep, tracing

13 Real-time estimation and dynamic renegotiation of UPC parameters for arbitrary traffic sources in ATM networks

Brian L. Mark, Gopalakrishnan Ramamurthy

December 1998 **IEEE/ACM Transactions on Networking (TON)**, Volume 6 Issue 6

Full text available: pdf(424.49 KB) Additional Information: full citation, references, citings, index terms

Keywords: asynchronous transfer mode, quality of service, real-time estimation, resource allocation, traffic characterization

14 Transparent optimizations of overheads in optimistic simulations

Rajive L. Bagrodia, Wen-Toh Liao

December 1992 **Proceedings of the 24th conference on Winter simulation**

Full text available: pdf(864.19 KB) Additional Information: full citation, references, citings, index terms

15 Algorithmic foundations for a parallel vector access memory system

Binu K. Mathew, Sally A. McKee, John B. Carter, Al Davis

July 2000 **Proceedings of the twelfth annual ACM symposium on Parallel algorithms and architectures**

Full text available: pdf(221.23 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents mathematical foundations for the design of a memory controller subcomponent that helps to bridge the processor/memory performance gap for applications with strided access patterns. The Parallel Vector Access (PVA) unit exploits the regularity of vectors or streams to access them efficiently in parallel on a multi-bank SDRAM memory system. The PVA unit performs scatter/gather operations so that only the elements accessed by the application are tra ...

16 System Deadlocks

E. G. Coffman, M. Elphick, A. Shoshani

June 1971 **ACM Computing Surveys (CSUR)**, Volume 3 Issue 2

Full text available: pdf(895.58 KB) Additional Information: full citation, abstract, references, citings, index terms

A problem of increasing importance in the design of large multiprogramming systems is the, so-called, deadlock or deadly-embrace problem. In this article we survey the work that has been done on the treatment of deadlocks from both the theoretical and practical points of view.

17 An architecture for software-controlled data prefetching

Alexander C. Klaiber, Henry M. Levy

April 1991 **ACM SIGARCH Computer Architecture News , Proceedings of the 18th**

annual international symposium on Computer architecture, Volume 19 Issue 3
Full text available: pdf(1.16 MB) Additional Information: full citation, references, citings, index terms

18 Steady-state simulation of queueing processes: survey of problems and solutions
Krzysztof Pawlikowski
June 1990 **ACM Computing Surveys (CSUR)**, Volume 22 Issue 2
Full text available: pdf(4.75 MB) Additional Information: full citation, abstract, references, citings, index terms

For years computer-based stochastic simulation has been a commonly used tool in the performance evaluation of various systems. Unfortunately, the results of simulation studies quite often have little credibility, since they are presented without regard to their random nature and the need for proper statistical analysis of simulation output data. This paper discusses the main factors that can affect the accuracy of stochastic simulations designed to give insight into the steady-st ...

19 Locality in distributed computations
David K. Garnick, A. Toni Cohen
February 1988 **Proceedings of the 1988 ACM sixteenth annual conference on Computer science**
Full text available: pdf(1.06 MB) Additional Information: full citation, abstract, references, index terms

The defining characteristic of a distributed system is the (temporal) distance between components; communication time is non-trivial compared to processing time. Because of this, the design of efficient distributed computations involves trade-offs between maximizing the amount of parallelism and minimizing communication costs. We argue that any sort of centralized control, whether in user-level algorithms or at the systems level, impairs efficiency. We then introduce a scheme for automatic ...

20 Exploiting high-level coherence information to optimize distributed shared state
DeQing Chen, Chunqiang Tang, Brandon Sanders, Sandhya Dwarkadas, Michael L. Scott
June 2003 **ACM SIGPLAN Notices , Proceedings of the ninth ACM SIGPLAN symposium on Principles and practice of parallel programming**, Volume 38 Issue 10
Full text available: pdf(341.96 KB) Additional Information: full citation, abstract, references, index terms

InterWeave is a distributed middleware system that supports the sharing of strongly typed, pointer-rich data structures across a wide variety of hardware architectures, operating systems, and programming languages. As a complement to RPC/RMI, InterWeave facilitates the rapid development of maintainable code by allowing processes to access shared data using ordinary reads and writes.Internally, InterWeave employs a variety of aggressive optimizations to obtain significant performance improvements ...

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

The ACM Portal is published by the Association for Computing Machinery. Copyright © 2005 ACM, Inc.
Terms of Usage Privacy Policy Code of Ethics Contact Us

Useful downloads: Adobe Acrobat QuickTime Windows Media Player Real Player

PORTAL
US Patent & Trademark Office

Subscribe (Full Service) Register (Limited Service, Free) Login

Search: The ACM Digital Library The Guide

plurality and media and writeable and concurrency and queues

THE ACM DIGITAL LIBRARY

Feedback Report a problem Satisfaction survey

Terms used
plurality and **media** and **writeable** and **concurrency** and **queues**

Found **5,276** of **150,885**

Sort results by: relevance
Display results: expanded form
Save results to a Binder
Search Tips
Open results in a new window

Try an Advanced Search
Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Best 200 shown

Relevance scale

1 The treatment of state in optimistic systems

David Bruce

July 1995 **ACM SIGSIM Simulation Digest , Proceedings of the ninth workshop on Parallel and distributed simulation**, Volume 25 Issue 1

Full text available: pdf(1.59 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Optimistic computation methods typically save copies of objects' state information, so that they can recover from erroneous "over-optimistic" computations. Such state saving is generally time and space consuming, and can be rather complicated both to implement and to use.I show how the data structure community's theory of persistence can be used not only to analyse and explain the treatment of state in optimistic systems, but also as a simple yet general mechanism for ...

Keywords: optimistic methods, parallel discrete event simulation, persistent data structures, state saving

2 Collaborative computing: a multi-client multi-server environment

Ming C. Hao, Alan H. Karp, Daniel Garfinkel

August 1995 **Proceedings of conference on Organizational computing systems**

Full text available: pdf(589.55 KB) Additional Information: full citation, abstract, references, citings, index terms

Most people think that collaboration implies that several people are sharing work on a single application with shared displays. In fact, collaboration is more. It includes the concurrent control of multiple applications by a collaborative group. To enable this more powerful form of collaboration, we show how to combine earlier mechanisms for single client, multiple server computing with a new mechanism called ESP (Event Sense Protocol) for multiple client, multiple server computing. We desc ...

3 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2

Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

4 A structural view of the Cedar programming environment 
Daniel C. Swinehart, Polle T. Zellweger, Richard J. Beach, Robert B. Hagmann
August 1986 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 8 Issue 4

Full text available: pdf(6.32 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents an overview of the Cedar programming environment, focusing on its overall structure—that is, the major components of Cedar and the way they are organized. Cedar supports the development of programs written in a single programming language, also called Cedar. Its primary purpose is to increase the productivity of programmers whose activities include experimental programming and the development of prototype software systems for a high-performance personal computer. T ...

5 Reference models, window systems, and concurrency 
K A Lantz, P P Tanner, C Binding, Kuan-Tsae Huang, A Dwelly
April 1987 **ACM SIGGRAPH Computer Graphics**, Volume 21 Issue 2

Full text available: pdf(1.30 MB) Additional Information: full citation, citings, index terms

6 Polling-based media access protocols for use with smart adaptive array antennas 
Srikanth V. Krishnamurthy, Anthony S. Acampora, Michele Zorzi
April 2001 **IEEE/ACM Transactions on Networking (TON)**, Volume 9 Issue 2

Full text available: pdf(271.34 KB) Additional Information: full citation, references, citings, index terms

Keywords: antenna, arrays, media, polling, protocols

7 The performance of multiversion concurrency control algorithms 
Michael J. Carey, Waleed A. Muhanna
September 1986 **ACM Transactions on Computer Systems (TOCS)**, Volume 4 Issue 4

Full text available: pdf(2.65 MB) Additional Information: full citation, abstract, references, citings, index terms

A number of multiversion concurrency control algorithms have been proposed in the past few years. These algorithms use previous versions of data items in order to improve the level of achievable concurrency. This paper describes a simulation study of the performance of several multiversion concurrency control algorithms, investigating the extent to which they provide increases in the level of concurrency and also the CPU, I/O, and storage costs resulting from the use of multiple versions. T ...

8 Concurrency and distribution in object-oriented programming 
Jean-Pierre Briot, Rachid Guerraoui, Klaus-Peter Lohr
September 1998 **ACM Computing Surveys (CSUR)**, Volume 30 Issue 3

Full text available: pdf(289.34 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper aims at discussing and classifying the various ways in which the object paradigm is used in concurrent and distributed contexts. We distinguish among the library approach, the integrative approach, and the reflective approach. The library approach applies object-oriented concepts, as they are, to structure concurrent and distributed systems through class libraries. The integrative approach consists of merging concepts such as obj ...

Keywords: concurrency, distribution, integration, libraries, message passing, object, reflection

9 ARIES: a transaction recovery method supporting fine-granularity locking and partial rollbacks using write-ahead logging

C. Mohan, Don Haderle, Bruce Lindsay, Hamid Pirahesh, Peter Schwarz
March 1992 **ACM Transactions on Database Systems (TODS)**, Volume 17 Issue 1

Full text available: pdf(5.23 MB) Additional Information: full citation, abstract, references, citings, index terms, review

DB2TM, IMS, and TandemTM systems. ARIES is applicable not only to database management systems but also to persistent object-oriented languages, recoverable file systems and transaction-based operating systems. ARIES has been implemented, to varying degrees, in IBM's OS/2TM Extended Edition Database Manager, DB2, Workstation Data Save Facility/VM, Starburst and QuickSilver, and in the University of Wisconsin's EXODUS and Gamma d ...

Keywords: buffer management, latching, locking, space management, write-ahead logging

10 Network Games: Consistency control for distributed interactive media

Jürgen Vogel, Martin Mauve
October 2001 **Proceedings of the ninth ACM international conference on Multimedia**

Full text available: pdf(444.23 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we present a generic consistency control service for distributed interactive media, i.e. media which allow a distributed group of users to interact with the medium itself. Consistency control is vital to these media since they typically require that a local copy of the medium's state be maintained by each user's application. Our service helps the applications to keep the local state copies consistent. The main characteristics of this service are as follows: a significant number of ...

Keywords: RTP/I, consistency, distributed interactive media, intention conflict, late join, local lag, mlb, timewarp

11 A comparison of high-availability media recovery techniques

George Copeland, Tom Keller
June 1989 **ACM SIGMOD Record , Proceedings of the 1989 ACM SIGMOD international conference on Management of data**, Volume 18 Issue 2

Full text available: pdf(1.32 MB) Additional Information: full citation, abstract, references, citings, index terms

We compare two high-availability techniques for recovery from media failures in database systems. Both techniques achieve high availability by having two copies of all data and indexes, so that recovery is immediate. "Mirrored declustering" spreads two copies of each relation across two identical sets of disks. "Interleaved declustering" spreads two copies of each relation across one set of disks while keeping both copies of each tuple on separate disks. Both ...

12 Specification and implementation of resilient, atomic data types
William Weihl, Barbara Liskov
June 1983 **Proceedings of the 1983 ACM SIGPLAN symposium on Programming language issues in software systems**
Full text available: pdf(1.28 MB) Additional Information: full citation, abstract, references, citings, index terms

A major issue in many applications is how to preserve the consistency of data in the presence of concurrency and hardware failures. We suggest addressing this problem by implementing applications in terms of abstract data types with two properties: Their objects are atomic (they provide serializability and recoverability for activities using them) and resilient (they survive hardware failures with acceptably high probability). We define what it means for abstract data types to be atomic and ...

13 Efficient user-space protocol implementations with QoS guarantees using real-time upcalls
R. Gopalakrishnan, Gurudatta M. Parulkar
August 1998 **IEEE/ACM Transactions on Networking (TON)**, Volume 6 Issue 4
Full text available: pdf(205.42 KB) Additional Information: full citation, references, citings, index terms

Keywords: multimedia communication, networks, operating system kernals, processor scheduling, protocols, real-time systems, transport protocols

14 Real-time computing with lock-free shared objects
James H. Anderson, Srikanth Ramamurthy, Kevin Jeffay
May 1997 **ACM Transactions on Computer Systems (TOCS)**, Volume 15 Issue 2
Full text available: pdf(390.82 KB) Additional Information: full citation, abstract, references, index terms

This article considers the use of lock-free shared objects within hard real-time systems. As the name suggests, lock-free shared objects are distinguished by the fact that they are accessed without locking. As such, they do not give rise to priority inversions, a key advantage over conventional, lock-based object-sharing approaches. Despite this advantage, it is not immediately apparent that lock-free shared objects can be employed if tasks must adhere to strict timing cons ...

Keywords: critical sections, deadline monotonic, earliest deadline first, hard real time, lock free, rate monotonic, scheduling, synchronization, wait free

15 Performance optimization for parallel tape arrays
Tzi-cker Chiueh
July 1995 **Proceedings of the 9th international conference on Supercomputing**
Full text available: pdf(958.52 KB) Additional Information: full citation, references, index terms

16 Ordered shared locks for real-time databases
Divyakant Agrawal, Amr El Abbadi, Richard Jeffers, Lijing Lin
January 1995 **The VLDB Journal — The International Journal on Very Large Data Bases**, Volume 4 Issue 1
Full text available: pdf(2.11 MB) Additional Information: full citation, abstract, references

We propose locking protocols for real-time databases. Our approach has two main motivations: First, locking protocols are widely accepted and used in most database systems. Second, in real-time databases it has been shown that the blocking behavior of transactions in locking protocols results in performance degradation. We use a new relationship between locks called ordered sharing to eliminate blocking that arises in the traditional locking protocols. Ordered sharing eliminates blocking of read ...

Keywords: concurrency control, time-critical scheduling, transaction management

17 Computing curricula 2001

September 2001 **Journal on Educational Resources in Computing (JERIC)**

Full text available: pdf(613.63 KB) html(2.78 KB) Additional Information: full citation, references, citings, index terms

18 PACT 2001 workshops. MediaBreeze: a decoupled architecture for accelerating multimedia applications

Deependra Talla, Lizy K. John

December 2001 **ACM SIGARCH Computer Architecture News**, Volume 29 Issue 5

Full text available: pdf(651.39 KB) Additional Information: full citation, abstract, references, index terms

Decoupled architectures are fine-grain processors that partition the memory access and execute functions in a computer program and exploit the parallelism between the two functions. Although some concepts from the traditional decoupled access execute paradigm made its way into commercial processors, they encountered resistance in general-purpose applications because these applications are not very structured and regular. However, multimedia applications have recently become dominant workload on ...

Keywords: SIMD, access and execute mechanisms, decoupling, general-purpose processors, hardware accelerators, microprocessor design, multimedia, prefetching

19 Extended ephemeral logging: log storage management for applications with long lived transactions

John S. Keen, William J. Dally

March 1997 **ACM Transactions on Database Systems (TODS)**, Volume 22 Issue 1

Full text available: pdf(566.34 KB) Additional Information: full citation, references, index terms, review

Keywords: OLTP, disk management, logging, long transactions

20 Empirical performance evaluation of concurrency and coherency control protocols for database sharing systems

Erhard Rahm

June 1993 **ACM Transactions on Database Systems (TODS)**, Volume 18 Issue 2

Full text available: pdf(3.37 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Database Sharing (DB-sharing) refers to a general approach for building a distributed high performance transaction system. The nodes of a DB-sharing system are locally coupled via a high-speed interconnect and share a common database at the disk level. This is also known as a "shared disk" approach. We compare database sharing with the database partitioning

(shared nothing) approach and discuss the functional DBMS components that require new and coordinated solutions for DB-shar ...

Keywords: coherency control, concurrency control, database partitioning, database sharing, performance analysis, shared disk, shared nothing, trace-driven simulation

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

The ACM Portal is published by the Association for Computing Machinery. Copyright © 2005 ACM, Inc.
Terms of Usage Privacy Policy Code of Ethics Contact Us

Useful downloads: Adobe Acrobat QuickTime Windows Media Player Real Player

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore

Welcome
United States Patent and Trademark Office

Help FAQ Terms IEEE Peer Review Quick Links

Welcome to IEEE Xplore

- Home
- What Can I Access?
- Log-out

Table of Contents

- Journals & Magazines
- Conference Proceedings
- Standards

Search

- By Author
- Basic
- Advanced
- CrossRef

Member Services

- Join IEEE
- Establish IEEE Web Account
- Access the IEEE Member Digital Library

IEEE Enterprise

- Access the IEEE Enterprise File Cabinet

Print Format

Your search matched **4** of **1131693** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

offsets<and>monotonically increasing Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **Tracking analysis of the NLMS algorithm in the presence of both ran and cyclic nonstationarities**
Moinuddin, M.; Zerguine, A.;
Signal Processing Letters, IEEE , Volume: 10 , Issue: 9 , Sept. 2003
Pages:256 - 258

[Abstract] [PDF Full-Text (258 KB)] **IEEE JNL**

2 **Wide-band radiometry for remote sensing of oil films on water**
Brown, E.R.; McMahon, O.B.; Murphy, T.J.; Hogan, G.G.; Daniels, G.D.; Hove
Microwave Theory and Techniques, IEEE Transactions on , Volume: 46 , Issue 12 , Dec. 1998
Pages:1989 - 1996

[Abstract] [PDF Full-Text (240 KB)] **IEEE JNL**

3 **Tracking analysis of normalized adaptive algorithms**
Moinuddin, M.; Zerguine, A.;
Acoustics, Speech, and Signal Processing, 2003. Proceedings. (ICASSP '03). 2 IEEE International Conference on , Volume: 6 , 6-10 April 2003
Pages:VI - 637-40 vol.6

[Abstract] [PDF Full-Text (285 KB)] **IEEE CNF**

4 **The performance choice: a study of chip and package densities**
Davidson, E.E.;
Electronic Components and Technology Conference, 1990. Proceedings., 40th 23 May 1990
Pages:147 - 151 vol.1

[Abstract] [PDF Full-Text (320 KB)] **IEEE CNF**

Copyright © 2004 IEEE — All rights reserved

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore

Welcome
United States Patent and Trademark Office

Help FAQ Terms IEEE Peer Review Quick Links

Welcome to IEEE Xplore

- Home
- What Can I Access?
- Log-out

Tables of Contents

- Journals & Magazines
- Conference Proceedings
- Standards

Search

- By Author
- Basic
- Advanced
- CrossRef

Member Services

- Join IEEE
- Establish IEEE Web Account
- Access the IEEE Member Digital Library

IEEE Enterprise

- Access the IEEE Enterprise File Cabinet

Your search matched **0** of **1131693** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

offsets<and>monotonically increasing<and>sequence Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

Results:
No documents matched your query.

Print Format

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ | Terms | Back to Top

Copyright © 2004 IEEE — All rights reserved

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore

Welcome
United States Patent and Trademark Office

Help FAQ Terms IEEE Peer Review Quick Links

Welcome to IEEE Xplore

- Home
- What Can I Access?
- Log-out

Tables of Contents

- Journals & Magazines
- Conference Proceedings
- Standards

Search

- By Author
- Basic
- Advanced
- CrossRef

Member Services

- Join IEEE
- Establish IEEE Web Account
- Access the IEEE Member Digital Library

IEEE Enterprise

- Access the IEEE Enterprise File Cabinet

Your search matched **0** of **1131693** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

first queue<and>recall request Search

Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

Results:
No documents matched your query.

Print Format

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ | Terms | Back to Top

Copyright © 2004 IEEE — All rights reserved

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore RELEASE 1.8

Welcome
United States Patent and Trademark Office

Help FAQ Terms IEEE Peer Review Quick Links

Welcome to IEEE Xplore
- Home
- What Can I Access?
- Log-out

Tables of Contents
- Journals & Magazines
- Conference Proceedings
- Standards

Search
- By Author
- Basic
- Advanced
- CrossRef

Member Services
- Join IEEE
- Establish IEEE Web Account
- Access the IEEE Member Digital Library

IEEE Enterprise
- Access the IEEE Enterprise File Cabinet

Your search matched **0** of **1131693** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

plurality request<and>data objects<and>migration<and Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

Results:
No documents matched your query.

Print Format

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ | Terms | Back to Top

Copyright © 2004 IEEE — All rights reserved

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore RELEASE 1.9

Welcome
United States Patent and Trademark Office

» Se

Help FAQ Terms IEEE Peer Review Quick Links

Welcome to IEEE Xplore

- Home
- What Can I Access?
- Log-out

Tables of Contents

- Journals & Magazines
- Conference Proceedings
- Standards

Search

- By Author
- Basic
- Advanced
- CrossRef

Member Services

- Join IEEE
- Establish IEEE Web Account
- Access the IEEE Member Digital Library

IEEE Enterprise

- Access the IEEE Enterprise File Cabinet

Your search matched **0** of **1131693** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

plurality request<and>migration<and>queues Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

Results:
No documents matched your query.

Print Format

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ | Terms | Back to Top

Copyright © 2004 IEEE — All rights reserved

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore RELEASE 1.8

Welcome
United States Patent and Trademark Office

» Se

Help FAQ Terms IEEE Peer Review Quick Links

Welcome to IEEE Xplore

- Home
- What Can I Access?
- Log-out

Tables of Contents

- Journals & Magazines
- Conference Proceedings
- Standards

Search

- By Author
- Basic
- Advanced
- CrossRef

Member Services

- Join IEEE
- Establish IEEE Web Account
- Access the IEEE Member Digital Library

IEEE Enterprise

- Access the IEEE Enterprise File Cabinet

Your search matched **0** of **1131693** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

plurality media and writeable and concurrency and quei Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

Results:
No documents matched your query.

Print Format

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ | Terms | Back to Top

Copyright © 2004 IEEE — All rights reserved

STIC Search Report
EIC 2100

STIC Database Tracking Number: 146227

TO:	From:
Fred Ehichoya **Location: RND 3B31** **Art Unit : 2162** **Monday, February 28, 2005** **Case Serial Number: 09/783820**	**Geoffrey St. Leger** **Location: EIC 2100** **Randolph-4B31** **Phone: 23450** **geoffrey.stleger@uspto.gov**

Search Notes

Dear Examiner Ehichoya,

Attached please find the results of your search request for application 09/783820. I searched Dialog's patent files and general files; along with the Internet.

Please let me know if you have any questions.

Regards,

Geoffrey St. Leger
4B30/308-7800

STIC EIC 2100 Search Request Form

146227

Today's Date: 2/28/05

What date would you like to use to limit the search?

Priority Date: 2/15/2001 Other:

Name FRED EHICHUYA

AU 2162 Examiner # 79719

Room # RAN 3B31 Phone 2-4034

Serial # 09/783820

Format for Search Results (Circle One):

(PAPER) DISK EMAIL

Where have you searched so far?

USP DWPI EPO JPO ACM IBM TDB

IEEE INSPEC SPI Other _____

Is this a "Fast & Focused" Search Request? (Circle One) (YES) NO

A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at http://ptoweb/patents/stic/stic-tc2100.htm.

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

CONCURRENT DATA RECALL IN A HIERARCHICAL STORAGE ENVIRONMENT USING PLURAL QUEUES.

- wherein each queued request indicates the offset from a predetermined location on a medium at which the requested data object is located, and wherein said placing act comprises:
- Organizing the request on each queue in a first and second sequence, each sequence comprising a set of request whose offsets are monotonically increasing within the respective sequence
- and wherein the act of creating a plurality of queues comprising timestamping each of the created queues, and wherein the act of activating a first of said plurality of queues comprises selecting a queue to be activated based on the timestamps of the respective queues.

STIC Searcher Geoffrey St. Leger Phone 23540

Date picked up 2/28/5 Date Completed 2/28/5

Search and Information Resources Administration

Warning: This HTML rendition of the RFC is experimental. It is programmatically generated, and small parts may be missing, damaged, or badly formatted. However, it is much more convenient to read via web browsers. Refer to the PostScript or text renditions for the ultimate authority.

The Open Group J. Bowe (TOG)
Request For Comments: 99.0 J. Salamone (TOG)
March 1997

MESSAGE QUEUING FOR DCE

INTRODUCTION

Providing a means for applications to communicate is a fundamental service of any distributed computing infrastructure. One method, which is analogous to inter-process communication mechanisms typically available within a single system, is message exchange. A message is a unit of data that one application process may send to other application processes. The size, content and significance of a message is determined by the communicating application processes.

DCE has always offered Remote Procedure Call (RPC) based communication. Some DCE-detractors claim that message passing and/or queuing is superior. We feel this sometimes turns into a religious battle. Our view is that it depends on the application. Providing some message-oriented services will make DCE more attractive for some application writers.

RFC 95, *DCE/NEXT: REQUIREMENTS SUMMARY*, asks for "support for message queuing in DCE and "support for messaging in DCE, including asynchronous RPC".

A prototype of this Message-Oriented Services package was shipped with DCE 1.2.2 in the unsupported area, ./src/nosupport/messaging in January 1997. Functionality includes most of the message queuing features outlined here.

Some Background on Messaging

Viewed from the highest level, there are three components of interest in the messaging environment: those that use the messaging service; those that the messaging service uses; and the messaging service itself. Each of these will be described in more detail in later sections.

There are primarily two types of message service users: senders and recipients of messages; and administrators. A sender is a process which calls upon the messaging service to communicate a message to other processes. A recipient is a process which calls upon the messaging service to retrieve messages that were sent by other processes. A process may be both a sender and a receiver. An

administrator controls the configuration and operation of the messaging service. The services provided by the messaging system to support these usage types are each described separately.

The messaging system itself provides services through two interfaces, one for message communication and related functions, and one for administration. Internally, the system is logically partitioned into the components which support the interfaces local to an individual system, queue managers, and queues. There may be multiple instances of each of these components as described later.

The messaging system makes use of data transmission, marshaling, naming, and security services provided by the underlying computing environment, in this case, DCE.

The messaging service allows senders and receivers to execute concurrently and to send and receive messages asynchronously. Two forms of asynchronous message communication to consider are message queuing and message passing. The focus of this work is to build a message queuing system, therefore, message passing will only be mentioned to illustrate some of the differences between queuing versus passing. To adequately describe these forms of message communication, some of the components of the messaging system must first be described in more detail.

Document Structure

The remainder of this document is divided into four sections. Section 2 describes some terminology. Section 3 describes the major goals of the project. Section 4 describes the network data structures Section 5 describes the RPC interfaces. Section 6 describes the API. Section 7 describes the administrative interface.

TERMINOLOGY

A "queue" is a container for 0 or more messages.

"Message queuing" is the exchange of messages between a sender and recipient through a third party. Sender and recipient processes need not be active at the same time.

"Message passing" is the exchange of messages between a sender and recipient directly. Sender and recipient processes must not be active at the same time.

A "queue manager" is a DCE server that manages a collection of queues. Message queuing requires a queue manager.

"Persistence" is how a message is stored within a queue manager. "Volatile" means it is stored in memory; this means it may be lost when the qeueue manager process exits. "Persistent" means it is stored in a stable place, typically on disk; this means it is not lost when the qeueue manager process exits and is restarted. We will use the DCE backing store library for persistent storage.

GOALS AND NON-GOALS

The following are the goals of this project:

a. Provide an infrastructure for secure message queuing between the queue manager and senders and recipients.
b. Implement on top of commercial DCE releases (OSF release 1.1). This means the DCE source is not a requirement.
c. Supply a set of APIs that let a user send an arbitrarily complex data structure to be to a destination.

The following are **not** goals:

a. Provide message passing.
b. Transaction capability.

System Features

The following is a list of queuing system features we will provide.

a. Adheres to the DCE security model. In addition, the API provides an interface for an end-to-end protection level and a means to identify initial senders to recipients.
b. An easy way to encode and decode (marshal) structured data as the message. This will be done with the existing RPC encoding services.
c. Uses the DCE namespace to identify queue managers and queues.
d. Automatic acknowledgement of message receipt (or dequeue)
e. Support the following attributes on queues
 i. queue name
 ii. queue name aliases
 iii. annotation
 iv. creation timestamp
 v. maximum message size
 vi. maximum length of queue
 vii. enable and disable of enqueue and dequeue operations
 viii. current length
 ix. last activity timestamp
 x. idle timeout for empty queues
 xi. persistence
f. Support the following attributes on messages
 i. unique message identifier (UUID)
 ii. enqueue timestamp
 iii. message type
 iv. data type (UUID)
 v. priority
 vi. message expiration
 vii. persistence
 viii. message sender (principal identity)
 ix. message delivery notice options
 x. end-to-end protection level (none, authentication, integrity, packet-level privacy)

g. Dequeue filtering based on some of the above message attributes

DATA STRUCTURES

Included here are the "major" data structures, as defined in various idl files. Minor, supporting types and enumerations are not shown.

This is the attribute structure of an individual message.

```
typedef struct mos_mattr_s_t {
    uuid_t          id;             /* ID of this item in the queue */
    uuid_t          datatype;       /* manager that encoded it */
    mos_msg_attr_msgtype_t
                    msgtype;        /* message type */
    sec_id_pa_t     sender;         /* sender identity */
    unsigned32      priority;       /* priority */
    unsigned32      flags;          /* flags */
    mos_msg_attr_persistence_t
                    persistence;
    /* notice_dest, notice_sec may be null */
    unsigned32      notice_opts;    /* notice options */
    [ptr,string]
      char          *notice_dest;   /* name of ack/reply queue */
    [ptr,string]
      char          *notice_sec_name;
                                    /* sec group other qmgr must be in */
    unsigned32      protectlvl;     /* protection level */
    /* want a counter instead of time enqueued? */
    utc_t           time_enqueued;  /* when msg was enqueued by q-mgr */
    utc_t           expire_time;    /* when this msg will expire */
    utc_t           valid_time;     /* when this msg will become valid */
    uuid_t          qid;            /* ID of queue where this lives */
} mos_mattr_t;
```

This is an array of bytes, which, as far as the messaging system is concerned, is the message payload or body.

```
typedef struct {
   unsigned32          size;
   [ptr,size_is(size)]
   byte *              data;
} mos_datatype_bytearray_t;
```

This is an item in the queue, composed of the message attributes and the body.

```
typedef struct mos_qitem_s_t {
    mos_mattr_t                     mattr;
    mos_datatype_bytearray_t        body;
} mos_qitem_t;
```

This is the attribute structure of a queue.

```
typedef struct mos_qattr_s_t {
    uuid_t          id;             /* ID of the queue */
    [ptr,string]
      char          *name;          /* name of the queue */
    [ptr,string]
      char          *annotation;    /* annotation */
    mos_string_list_t
```

```
                    aliases;        /* alias names of the queue */
    mos_que_attr_persistence_t
                    persistence;
    boolean         enq_enabled;    /* enqueue: enable/disable */
    boolean         deq_enabled;    /* dequeue: enable/disable */
    unsigned32      flags;          /* flags */
    unsigned32      len;            /* current length of queue [ro] */
    unsigned32      max_msgsize;    /* max message size */
    unsigned32      max_qlen;       /* max length of queue */
    utc_t           created;        /* time created [ro] */
    utc_t           empty_timeout;  /* idle/empty time before removing */
    utc_t           last_activity;  /* time of last activity [ro] */
    uuid_t          acl;            /* ACL uuid - internal use [ro] */
} mos_qattr_t;
```

QUEUE MANAGER RPC OPERATIONS

Management (Queue Manager) Operations

mos_mgmt_create_queue()

Create a queue.

mos_mgmt_get_id_list()

Return a list of the IDs of all queues.

mos_mgmt_rename()

Rename a queue within queue manager.

mos_mgmt_move()

Move messages from one queue to another, retaining all attributes. This is within the same queue manager.

Queue (Data) Operations

mos_q_enqueue()

Enqueue a message in a given queue. The message is placed in the queue according to priority.

Queue Attribute Utilities

Client interfaces for Queue Attribute Utilities to support the Message Oriented Service Application Programming Interface(MOS-API).

mos_que_attr_alloc

Allocates memory within MOS and returns an opaque pointer to a queue attributes structure with defaults set.

```
void
mos_que_attr_alloc(
    /* [out] */         mos_que_attr_t *        que_attributes,
    /* [out] */         error_status_t *        status
);
```

mos_que_attr_peek

Returns an opaque pointer to the queue attributes on an existing queue.

```
void
mos_que_attr_peek(
    /* [in] */          mos_handle_t            resource_handle,
    /* [out] */         mos_que_attr_t *        que_attributes,
    /* [out] */         error_status_t *        status
);
```

mos_que_attr_free

Releases memory used for queue attributes. It is the responsibility of the caller to release the memory if allocated by mos_que_attr_alloc() or mos_que_attr_peek().

```
void
mos_que_attr_free(
    /* [in,out] */      mos_que_attr_t *        que_attributes,
    /* [out] */         error_status_t *        status
);
```

Commit queue attribute modifications on an existing queue.

```
void
mos_que_attr_commit(
    /* [in] */          mos_handle_t            resource_handle,
    /* [in] */          mos_que_attr_t          queue_attributes,
    /* [out] */         error_status_t *        status
);
```

mos_que_attr_queid_get

Return queue ID from queue attributes structure.

```
void
mos_que_attr_queid_get(
    /* [in] */          mos_que_attr_t          que_attributes,
    /* [out] */         uuid_t *                que_id,
    /* [out] */         error_status_t *        status
);
```

mos_que_attr_quecursize_get

Return current queue size from queue attributes structure.

```
void
mos_que_attr_quecursize_get(
    /* [in] */          mos_que_attr_t          que_attributes,
    /* [out] */         unsigned32 *            que_cur_size,
    /* [out] */         error_status_t *        status
);
```

mos_que_attr_createtime_get

Return queue creation time stamp in absolute time from queue attributes structure.

```
void
mos_que_attr_createtime_get(
    /* [in] */          mos_que_attr_t          que_attributes,
    /* [out] */         utc_t *                 que_create_time,
    /* [out] */         error_status_t *        status
);
```

mos_que_attr_activetime_get

Return queue last activity time stamp in absolute time from queue attributes structure.

```
void
mos_que_attr_activetime_get(
    /* [in] */          mos_que_attr_t          que_attributes,
    /* [out] */         utc_t *                 que_active_time,
    /* [out] */         error_status_t *        status
);
```

mos_que_attr_alias_list

Return the list of queue aliases by name from queue attributes structure. The first entry in the list is the queue name itself.

```
void
mos_que_attr_alias_list(
    /* [in] */          mos_que_attr_t          que_attributes,
    /* [in] */          unsigned32              space_avail,
```

```
File 347:JAPIO Nov 1976-2004/Oct(Updated 050208)
         (c) 2005 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200513
         (c) 2005  Thomson Derwent

Set     Items   Description
S1     251471   QUEUE? ? OR BUFFER? ?
S2     108144   (ORGANIZ? OR ORGANIS? OR SORT??? OR ORDER??? OR SHUFFL??? -
             OR ARRANG? OR PRIORITIZ? OR PRIORITIS?)(5N)(REQUEST? ? OR QUE-
             RY OR QUERIES OR TRANSACTION? ? OR TASK? ? OR ITEM? ? OR DATA
             OR INFORMATION OR ADDRESS OR ADDRESSES)
S3       8026   (ORGANIZ? OR ORGANIS? OR SORT??? OR ORDER??? OR SHUFFL??? -
             OR ARRANG? OR PRIORITIZ? OR PRIORITIS?)(5N)(POINTER? ? OR TAS-
             K? ? OR JOB? ? OR INSTRUCTION? ?)
S4       5157   (RESORT? OR REPRIORITIZ? OR REPRIORITIS? OR REQUEU? OR REO-
             RDER? OR RESEQUENC? OR REARRANG? OR REORGANI? OR RESHUFFL?)(5-
             N)(REQUEST? ? OR QUERY OR QUERIES OR TRANSACTION? ? OR TASK? ?
              OR ITEM? ? OR DATA OR INFORMATION OR ADDRESS??)
S5        406   (RESORT? OR REPRIORITIZ? OR REPRIORITIS? OR REQUEU? OR REO-
             RDER? OR RESEQUENC? OR REARRANG? OR REORGANI? OR RESHUFFL?)(5-
             N)(POINTER? ? OR TASK? ? OR JOB? ? OR INSTRUCTION? ?)
S6     185736   (SEQUENCE? ? OR SERIES OR PATTERN? ? OR GROUP? ? OR CLUSTE-
             R? ?)(7N)(REQUEST? ? OR QUERY OR QUERIES OR TRANSACTION? ? OR
             TASK? ? OR ITEM? ? OR DATA OR INFORMATION OR ADDRESS OR ADDRE-
             SSES OR POINTER?? OR TASK? ? OR JOB? ? OR INSTRUCTION? ?)
S7    3937105   MEDIUM OR MEDIA OR STORAGE OR TAPE? ? OR CASSETTE? ? OR DI-
             SK? ? OR DISC? ? OR DRIVE? ? OR CD OR CDROM OR DVD
S8     149075   OFFSET? ? OR OFF()SET? ?
S9       1899   MONOTONIC?
S10       115   S1(5N)(TIMESTAMP? OR TIME()STAMP?)
S11      7608   S1 AND S2:S5
S12      4476   S11 AND IC=G06F
S13      1263   S11 AND S6
S14       526   S13 AND S7
S15         7   S14 AND S8:S9
S16         2   AU=KALACH R?
S17     71389   S1(7N)(REQUEST? ? OR QUERY OR QUERIES OR TRANSACTION? ? OR
             TASK? ? OR ITEM? ? OR DATA OR INFORMATION OR ADDRESS?? OR POI-
             NTER? ? OR TASK? ? OR JOB? ? OR INSTRUCTION? ?)
S18      5756   S17 AND S2:S5
S19       976   S18 AND S6
S20        53   S18 AND S8:S9
S21        49   S20 NOT S15
S22        24   S21 AND AC=US/PR
S23        23   S22 AND AY=(1970:2001)/PR
S24        39   S21 AND PY=1970:2001
S25        40   S23:S24
S26    236342   S7(10N)(RETRIEV? OR OBTAIN??? OR RECALL??? OR LOAD??? OR R-
             EQUEST??? OR FETCH???)
S27       307   S18 AND S26
S28        67   S6 AND S27
S29        65   S28 NOT (S15 OR S21)
S30    394681   TAPE OR TAPES OR CASSETTE? ?
S31    804810   HEAD? ? OR TAPEHEAD? ? OR DRIVEHEAD? ? OR DISCHEAD? ? OR D-
             ISKHEAD? ?
S32       140   S18 AND S30
S33        11   S32 AND S26
S34      2731   S1(7N)S2:S5
S35        56   S32 AND S34
S36        64   S33 OR S35
S37        62   S36 NOT (S15 OR S21 OR S29)
S38        13   S37 AND AC=US/PR
S39        13   S38 AND AY=(1970:2001)/PR
S40        56   S37 AND PY=1970:2001
S41        60   S39:S40
S42        27   S32 AND S31
S43        11   S42 NOT (S15 OR S21 OR S29 OR S37)
S44      2938   REQUEST? ?(3N)(ORGANIZ? OR ORGANIS? OR SORT??? OR ORDER???
```

OR SHUFFL??? OR ARRANG? OR PRIORITIZ? OR PRIORITIS?)

S45	203	S1(10N)S44
S46	27	S45 AND S6
S47	21	S46 NOT (S15 OR S21 OR S29 OR S37)

15/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

03354968 **Image available**
HARD **DISK** CONTROL METHOD

PUB. NO.: 03-017868 [JP 3017868 A]
PUBLISHED: January 25, 1991 (19910125)
INVENTOR(s): IIIZUMI TOMOO
APPLICANT(s): ALPS ELECTRIC CO LTD [001009] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-150393 [JP 89150393]
FILED: June 15, 1989 (19890615)
INTL CLASS: [5] G11B-020/12
JAPIO CLASS: 42.5 (ELECTRONICS -- Equipment)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: P, Section No. 1188, Vol. 15, No. 140, Pg. 81, April 09, 1991 (19910409)

ABSTRACT

PURPOSE: To shorten a time to read out data from a **disk** by performing readout from a sector immediately after generating a readout command, setting a **storage** address by using **address information** , and performing **data arrangement** on a memory.

CONSTITUTION: ID information is read out, and a DMA address is generated at a DMA start address register 5 setting a sector number and sector length as **offsets** if the ID information is the one on an unread sector, and it is sent to a sector **buffer** 7, and reading from the sector is performed immediately after receiving a read instruction, and the **storage** address in the memory of a transfer destination is designated by conforming to the sector number, also, a preceding sector before than a read sector is read with the next rotation and is transferred to and stored at an address position calculated with calculation of (sector number X sector length), thereby, the **data** is read in **sequence** according to **data sequence** on a track, and is arranged in the sector **buffer** 7.

25/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

06397133 **Image available**
INFORMATION STORAGE DEVICE AND CORRECTED ADDRESS GENERATING METHOD

PUB. NO.: 11-338784 [JP 11338784 A]
PUBLISHED: December 10, 1999 (**19991210**)
INVENTOR(s): TAKAHASHI KOJI
NISHITANI TAKUJI
OGAWA HITOSHI
YAMAMOTO KATSUMI
NISHINA MASATOSHI
APPLICANT(s): HITACHI LTD
APPL. NO.: 10-139589 [JP 98139589]
FILED: May 21, 1998 (19980521)
INTL CLASS: G06F-012/16; G06F-011/10

ABSTRACT

PROBLEM TO BE SOLVED: To provide a magnetic disk device capable of improving error correction ability by prolonging time for accessing a **data buffer** when correcting one sector **data** through an error correcting part.
SOLUTION: A base address for each sector is successively held in an EDC base address register 100. At the time of error correction, a subtracter 103 generates a corrected address showing a position to be corrected from the held base address and an **offset** address showing the error position in the sector. The error correcting part corrects the error of read information for each sector. Corresponding to a sector OK signal 107 which is outputted when the error correction for each sector is completed or there is no error, according to the predetermined **order** for each sector, an **address** generating part 10 updates the base address.

COPYRIGHT: (C)1999,JPO

25/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

05696977 **Image available**
DATA TRANSFER CONTROLLER

PUB. NO.: 09-311777 [JP 9311777 A]
PUBLISHED: December 02, 1997 (**19971202**)
INVENTOR(s): OGAWA TAKAHISA
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-127542 [JP 96127542]
FILED: May 22, 1996 (19960522)
INTL CLASS: [6] G06F-005/06
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JAPIO KEYWORD:R129 (ELECTRONIC MATERIALS -- Super High Density Integrated Circuits, LSI & GS

ABSTRACT

PROBLEM TO BE SOLVED: To reduce the information amount and to greatly reduce the load on process by dividing a data area into area units and assigning block numbers, and setting a block number for starting data transfer in table data generated in a transfer parameter storage area.
SOLUTION: The transfer parameter storage area is provided on the low-**order address** side of a **buffer** memory and a **data** area is provided on the high-**order address** side. The transfer parameter storage area is divided into a disk-side transfer parameter storage area and a host-side transfer parameter storage area. The data area is divided into arbitrary area units set in an area unit setting regster from an arbitrary **offset**

address set in an **offset** address setting register, and a numbers are assigned to the divided areas in the order of, for example, block 1, a block 2... a block (n).

25/5/10 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

014885008 **Image available**
WPI Acc No: 2002-705714/200276
XRPX Acc No: N02-556304
Demultiplexer for digital satellite broadcast receiver, writes subsequent data packet retrieval from packet buffer into new location offset from location assigned to previously retrieval packet, for storing new data
Patent Assignee: COUPE D (COUP-I); FOSTER E M (FOST-I); LLOYD B J (LLOY-I); NGAI C H (NGAI-I); INT BUSINESS MACHINES CORP (IBMC)
Inventor: COUPE D; FOSTER E M; LLOYD B J; NGAI C H
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020067745	A1	20020606	US 2000730636	A	20001206	200276 B
US 6831931	B2	20041214	US 2000730636	A	20001206	200501

Priority Applications (No Type Date): US 2000730636 A 20001206
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020067745	A1		9	H04J-003/04	
US 6831931	B2			H04J-003/02	

Abstract (Basic): US 20020067745 A1
NOVELTY - A data unloader (28) writes successive transport stream packets retrieval from a packet **buffer** into contiguous **address** locations in a memory. A remultiplexer **arrangement** writes the next **data** packet retrieved from the **buffer** into new location **offset** from location assigned to previous packet, so as to write new data content in the **offset** location.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for data packets remultiplexing method.
USE - Demultiplexer for digital satellite broadcast receiver, demultiplexing audio and video data streams.
ADVANTAGE - Enables insertion of new data content into the gap created in the memory and remultiplexes the transport stream effectively.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of demultiplexer.
Data unloader (28)
pp; 9 DwgNo 1/3
Title Terms: DEMULTIPLEXER; DIGITAL; SATELLITE; BROADCAST; RECEIVE; WRITING ; SUBSEQUENT; DATA; PACKET; RETRIEVAL; PACKET; BUFFER; NEW; LOCATE; **OFFSET** ; LOCATE; ASSIGN; RETRIEVAL; PACKET; STORAGE; NEW; DATA
Derwent Class: W01; W02; W03
International Patent Class (Main): H04J-003/02; H04J-003/04
File Segment: EPI

25/5/13 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

013522358 **Image available**
WPI Acc No: 2001-006564/ **200101**
Related WPI Acc No: 1999-494638; 2001-006562; 2001-006563; 2001-006565; 2001-006566; 2001-476082; 2001-662471; 2002-040650; 2002-147020; 2002-154139; 2002-171041; 2002-266949; 2002-392459; 2002-392482; 2003-331244; 2003-401569; 2003-709043; 2004-345168; 2004-439776
XRPX Acc No: N01-004715

Computer graphics system filters the samples stored in buffer **, based on position** information **in** order **to generate output pixels for display**

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: DEERING M F
Number of Countries: 090 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200049576	A1	20000824	WO 2000US4147	A	20000217	200101	B
AU 200032355	A	20000904	AU 200032355	A	20000217	200103	
EP 1155385	A1	20011121	EP 2000910228	A	20000217	200176	
			WO 2000US4147	A	20000217		
KR 2002031097	A	20020426	KR 2001709656	A	20010731	200270	
EP 1155385	B1	20021030	EP 2000910228	A	20000217	200272	
			WO 2000US4147	A	20000217		
DE 6020000681	E	20021205	DE 2000600681	A	20000217	200304	
			EP 2000910228	A	20000217		
			WO 2000US4147	A	20000217		
JP 2003529115	W	20030930	JP 2000600240	A	20000217	200365	
			WO 2000US4147	A	20000217		

Priority Applications (No Type Date): US 99413106 A 19991006; US 99251453 A 19990217
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200049576	A1	E	54	G06T-015/50	
Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW					
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW					
AU 200032355	A				Based on patent WO 200049576
EP 1155385	A1	E			Based on patent WO 200049576
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
KR 2002031097	A			G06T-015/00	
EP 1155385	B1	E		G06T-015/50	Based on patent WO 200049576
Designated States (Regional): DE FR GB IE NL					
DE 6020000681	E			G06T-015/50	Based on patent EP 1155385
					Based on patent WO 200049576
JP 2003529115	W		91	G06T-005/20	Based on patent WO 200049576

Abstract (Basic): WO 200049576 A1

NOVELTY - A processor (352) which renders one or more samples, is coupled to sample buffer (162) which stores the samples. Each sample corresponds to position information having one or more **offset** values. A sample-to-pixel calculator (360) coupled to buffer is operable to filter samples in **buffer** , based on position **information** in **order** to generate output pixels for display.

DETAILED DESCRIPTION - The **offset** values are relative to one or more predefined screen space locations or predefined grid. An INDEPENDENT CLAIM is also included for method for generating pixels for display in graphics system.

USE - Computer graphics system.

ADVANTAGE - Enables to generate and store more than one sample for a subset of pixel locations on display, thus provides a super sampled sample buffer which stores a number of samples far greater than number of pixel locations on display. Performs calculation of each pixel for each screen refresh on real time basis or on an on-the-fly basis.

DESCRIPTION OF DRAWING(S) - The figure shows the computer graphic system with super sampled sample buffer.

Sample buffer (162)
Processor (352)
Sample-to-pixel calculator (360)
pp; 54 DwgNo 6A/14

Title Terms: COMPUTER; GRAPHIC; SYSTEM; FILTER; SAMPLE; STORAGE; BUFFER; BASED; POSITION; INFORMATION; ORDER; GENERATE; OUTPUT; PIXEL; DISPLAY
Derwent Class: T01

International Patent Class (Main): G06T-005/20; G06T-015/00; G06T-015/50
International Patent Class (Additional): G06T-011/00
File Segment: EPI

25/5/14 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

013465260 **Image available**
WPI Acc No: 2000-637203/ **200061**
Related WPI Acc No: 2001-540429; 2002-237666
XRPX Acc No: N00-472501

Direct memory access circuit has state machine to respond to jump instruction read by data transfer circuit by resetting value designating position of subsequent data **in** buffer **, to be copied to input-output devices**

Patent Assignee: NVIDIA CORP (NVID-N)
Inventor: IWAMOTO R; JOHNSON S; PRIEM C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6092124	A	20000718	US 9861719	A	19980417	200061	B

Priority Applications (No Type Date): US 9861719 A 19980417
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6092124	A		11	G06F-013/00	

Abstract (Basic): US 6092124 A

NOVELTY - A **data** transfer circuit reads **data** from **buffer** of system memory in a designated position to copy **information** from **buffer** to input-output device (16) in the sequence. A state machine (45) responds to the jump instruction read by data transfer circuit by causing the DMA circuit to reset the value determining position within **buffer** portion, from which subsequent **data** is to be copied to input-output device.

DETAILED DESCRIPTION - A direct memory access circuit (30) stores reference value pointing to **data** structure (36) describing a **buffer** portion of memory (37). The memory location is identified by an initial position with initial address. The final position has an address determined by the initial address and an **offset** value.

USE - For use with input-output devices to transfer graphics data from memory to graphics accelerator.

ADVANTAGE - The DMA circuit frees the central processor for other activities and hence increases the speed of data transfer from memory to input-output devices. In DMA circuit additional registers are also used for each additional transfer **buffers** . This allows the **data** transfer process to be overlapped and realizes rapid transfers. Large number of registers required in the conventional circuit is eliminated and the state machines required for operating the DMA engine is simplified. The need for CPU to weight for a notify signal before transferring or placing next sequence of data, is eliminated. This greatly increases the speed of data transfer. Use of jump instructions allow the DMA engine to handle advanced operations. Hence sequence of data is transferred with single command to the registers on the input-output device.

DESCRIPTION OF DRAWING(S) - The figure shows the **arrangement** of **data** transfer with DMA circuit.

Input-output device (16)
Memory access circuit (30)
Data structure (36)
Memory (37)
State machine (45)
pp; 11 DwgNo 2/5

Title Terms: DIRECT; MEMORY; ACCESS; CIRCUIT; STATE; MACHINE; RESPOND; JUMP ; INSTRUCTION; READ; DATA; TRANSFER; CIRCUIT; RESET; VALUE; DESIGNATED; POSITION; SUBSEQUENT; DATA; BUFFER; COPY; INPUT; OUTPUT; DEVICE

Derwent Class: T01
International Patent Class (Main): G06F-013/00
File Segment: EPI

25/5/24 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

011214516 **Image available**
WPI Acc No: 1997-192441/ **199717**
XRPX Acc No: N97-159038
Bundling client write requests in server - bundling together client write requests **that have been received in** queue **with current write** request **, according to whether set capacity of requests that are contiguous to current write** request **have been placed in** queue
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: BALDIGA F P; MEYER C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5613155	A	19970318	US 95475728	A	19950607	199717	B

Priority Applications (No Type Date): US 95475728 A 19950607
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5613155	A		24	G06F-013/00	

Abstract (Basic): US 5613155 A
The logic for receiving client requests is included in an intermediate server which includes a write request module having a write bundling module included and a write reply module. A separate reply is sent for each of the individual client write requests.
Out of **order requests** are handled by checking for a contiguous write having a lower file location (**offset**) than a current write **request** and placing that lower **ordered offset request** first in the bundle.
ADVANTAGE - Logic for receiving client write requests, bundling them, and sending reply back to client(s) once requests are committed to storage. Optimised performance of write operations.
Dwg.2/13
Title Terms: BUNDLE; CLIENT; WRITING; REQUEST; SERVE; BUNDLE; CLIENT; WRITING; REQUEST; RECEIVE; QUEUE; CURRENT; WRITING; REQUEST; ACCORD; SET; CAPACITY; REQUEST; CONTIGUOUS; CURRENT; WRITING; REQUEST; PLACE; QUEUE
Derwent Class: T01
International Patent Class (Main): G06F-013/00
File Segment: EPI

25/5/25 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

010868106 **Image available**
WPI Acc No: 1996-365057/ **199637**
XRPX Acc No: N96-307771
Data buffer **for transferring** data **between two processor - has decoder which selectively applies** offset **to addressing signals depending upon whether writing operation or reading operation is perform**
Patent Assignee: NOKIA CORP (OYNO); NOKIA MOBILE PHONES LTD (OYNO)
Inventor: FRAMPTON S
Number of Countries: 004 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2298109	A	19960821	GB 952823	A	19950214	199637	B
EP 729106	A1	19960828	EP 96300868	A	19960209	199639	
US 5802351	A	19980901	US 96596720	A	19960205	199842	
GB 2298109	B	19990901	GB 952823	A	19950214	199937	

EP 729106	B1	20030108	EP 96300868	A	19960209	200304
DE 69625631	E	20030213	DE 625631	A	19960209	200320
			EP 96300868	A	19960209	

Priority Applications (No Type Date): GB 952823 A 19950214
Cited Patents: 4.Jnl.Ref; JP 3081851; JP 3095916; JP 5303524; JP 60237566
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2298109	A		21	G06F-005/06	
EP 729106	A1	E	12	G06F-015/16	
Designated States (Regional): DE FR GB					
US 5802351	A			G06F-013/00	
GB 2298109	B			G06F-005/06	
EP 729106	B1	E		G06F-015/16	
Designated States (Regional): DE FR GB					
DE 69625631	E			G06F-015/16	Based on patent EP 729106

Abstract (Basic): GB 2298109 A

The **buffer** has a storage device **arranged** to buffer **data** signals generated by each processing device for reception by other processing device. A storage allocation device arranged to adjust the amount of storage provided by the storage device for transfer in each direction. A two-part random access memory has one port for data transfer with first processing device and a second port for data transfer with the second processing device.

An address generator generates addressing signals for writing of **data** to the **buffer** or reading **data** from the **buffer** . An **address** interpretation device enables the **address** generator in response to a particular addressing signal generated by the first or second processing device. A decoder selectively applies an **offset** to the addressing signals depending upon whether a writing operation or a reading operation is perform.

ADVANTAGE - Provides addressable storage area which may be **addressed** so as to **buffer data** generated by first processor, for transfer to second processor

Dwg.2/4

Title Terms: DATA; BUFFER; TRANSFER; DATA; TWO; PROCESSOR; DECODE; SELECT; APPLY; **OFFSET** ; ADDRESS; SIGNAL; DEPEND; WRITING; OPERATE; READ; OPERATE ; PERFORMANCE
Derwent Class: T01; W01
International Patent Class (Main): G06F-005/06; G06F-013/00; G06F-015/16
International Patent Class (Additional): G06F-009/38
File Segment: EPI

25/5/30 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

008712932 **Image available**
WPI Acc No: 1991-216951/ **199130**
XRPX Acc No: N91-165555

Burst and non-burst data router for communication system - has output frame buffers **for storing input** data **in deshuffled** order **and provides formatted and** shuffled **output** data

Patent Assignee: HUGHES AIRCRAFT CO (HUGA)
Inventor: CLEBOWICZ B A
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 438274	A	19910724	EP 91300297	A	19910116	199130	B
CA 2032955	A	19910717				199139	
JP 4212548	A	19920804	JP 912726	A	19910114	199237	
EP 438274	A3	19930303	EP 91300297	A	19910116	199349	
EP 438274	B1	19970618	EP 91300297	A	19910116	199729	
DE 69126551	E	19970724	DE 626551	A	19910116	199735	
			EP 91300297	A	19910116		

Priority Applications (No Type Date): US 90464794 A 19900116
Cited Patents: NoSR.Pub; 1.Jnl.Ref; EP 239937; WO 8809015
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 438274	A				
Designated States (Regional): DE FR GB IT					
JP 4212548	A		8		
EP 438274	B1	E	12		
Designated States (Regional): DE FR GB IT					
DE 69126551	E				Based on patent EP 438274

Abstract (Basic): EP 438274 A

The data router (10) performs input data deshuffling and outupt **data** formatting and **shuffling** and operates with both bursted and non-bursted input and output **data** , using only one small input **buffer** (14) per input channel (16) and one frame buffer per output channel (26).

The router includes input channels (16) for receiving input **data** , input burst **buffers** (14) for storing the input **data** , input **address** controllers (15) for providing input **data** storage information, output frame **buffers** (23) for storing the input **data** in a deshuffled **order** and providing formatted and **shuffled** output **data** , output channels (26) for transmitting the output data and a router controller (20) for controlling the operation of the router (10).

USE/ADVANTAGE - Especially for satellites. Requires less memory for input data deshuffling. (11pp Dwg.No.3/5

Title Terms: BURST; NON; BURST; DATA; ROUTER; COMMUNICATE; SYSTEM; OUTPUT; FRAME; BUFFER; STORAGE; INPUT; DATA; ORDER; SHUFFLE; OUTPUT; DATA
Derwent Class: W01
International Patent Class (Main): H04L-012/56
International Patent Class (Additional): H04Q-003/00
File Segment: EPI

29/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

06608750 **Image available**
ARITHMETIC PROCESSOR AND **INSTRUCTION ORDER** CONTROL METHOD

PUB. NO.: 2000-194555 [JP 2000194555 A]
PUBLISHED: July 14, 2000 (20000714)
INVENTOR(s): ASANO SHIGEHIRO
YOSHIKAWA YOSHIFUMI
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 10-373380 [JP 98373380]
FILED: December 28, 1998 (19981228)
INTL CLASS: G06F-009/38; G06F-009/30

ABSTRACT

PROBLEM TO BE SOLVED: To further improve frequency by judging whether or not a **fetched** instruction or an instruction stored in an instruction **storage** means can be executed according to information regarding the use states of registers.

SOLUTION: For example, when two pipeline units 6-1 and 6-2 are provided, this dynamic VLIW system is provided with independent Pending Queues 2-1 and 2-2 for slots 1 and 2, respectively, so as to save an **instruction** fetched from a normal **instruction sequence** as an execution waiting **instruction** if it can not be executed immediately. Further, out-of-order is realized by using a table called a score board 4 for managing information regarding the use states of the registers for each register. an atom which is not executed among atoms of a fetched VLIW **instruction** is saved in the Pending **Queues** 2-1 and 2-2 until its execution becomes possible.

COPYRIGHT: (C)2000,JPO

29/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

06462427 **Image available**
REAL TIME SHARED DISK SYSTEM FOR COMPUTER CLUSTER

PUB. NO.: 2000-048001 [JP 2000048001 A]
PUBLISHED: February 18, 2000 (20000218)
INVENTOR(s): DANIEL MANUEL DIAS
RAAJATO MUKERUJII
APPLICANT(s): INTERNATL BUSINESS MACH CORP (IBM)
APPL. NO.: 11-182660 [JP 99182660]
FILED: June 29, 1999 (19990629)
PRIORITY: 113752 [US 98113752], US (United States of America), July 10, 1998 (19980710)
INTL CLASS: G06F-015/16; G06F-012/00; G06F-015/177

ABSTRACT

PROBLEM TO BE SOLVED: To execute the issuance, updating and discontinuance of **data** access **requests** with priority **orders** for a shared **storage** system inside a clustered computer system by sequencing the data access **requests** in a **storage** node based on the respective priority orders.
SOLUTION: For respective **storage** computers 18, respective **request queues** 32 for which **data** read **requests** and **data** write **requests** are **sequenced** by the priority **orders** are provided. In the case that the element of the storage computer 18 is not a system disk controller, only one input/output operation is presented at one time to a relating data storage device 20. It is preferable that a normal time synchronizer 34 executed by software or hardware synchronizes the clock of a client

computer 12 and the storage computer 18. The priority order generally means the restriction of the data access request for performing limitation so as to respond to the **request** by using the respective priority **orders** by the system 10.

COPYRIGHT: (C)2000,JPO

29/5/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

06403439 **Image available**
DISK CONTROLLING METHOD AND DISK DEVICE

PUB. NO.: 11-345094 [JP 11345094 A]
PUBLISHED: December 14, 1999 (19991214)
INVENTOR(s): OKAMOTO KEIJI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD
APPL. NO.: 10-149848 [JP 98149848]
FILED: May 29, 1998 (19980529)
INTL CLASS: G06F-003/06

ABSTRACT

PROBLEM TO BE SOLVED: To shorten each seaking time and total access time by providing the method with a step for determining the access execution **order** of a succeeding access **request group** based on relation between a final **disk** head position and the **disk** head position of an access **request group** to be executed next and other steps.

SOLUTION: An access **request** queue 1 collects plural access **requests** as an access request **group** and sends the access **request group** to an access **request order rearranging** part 2. The **rearranging** part 2 mutually compares logical **address** values stored in a data **storage** device which are specified by respective access **requests** and **rearranges** the access **request order** in the ascending direction of logical **addresses** . Then the **rearranging** part 2 determines the execution **order** based on access execution history **data** taken out from an access request execution history storing part 5 and the **rearranged** access **request** order. An access **request** execution part 3 executes an access to the data **storage** device 4 in accordance with the access execution order determined by the rearranging part 2.

COPYRIGHT: (C)1999,JPO

29/5/4 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

05828662 **Image available**
STORAGE DEVICE SUB-SYSTEM

PUB. NO.: 10-111762 [JP 10111762 A]
PUBLISHED: April 28, 1998 (19980428)
INVENTOR(s): YAMAMOTO YASUTOMO
YAMAMOTO AKIRA
SATO TAKAO
KITAMURA MANABU
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-266914 [JP 96266914]
FILED: October 08, 1996 (19961008)
INTL CLASS: [6] G06F-003/06; G06F-003/06; G06F-003/06; G06F-012/08; G06F-012/16
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 45.2 (INFORMATION PROCESSING -- Memory Units)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce the **load** of a **storage** controller, to improve efficiency by means of considering the locality and the characteristic of data access and to shorten seeking/searching time in a storage device.

SOLUTION: The storage controller 104 and a disk device 105 are connected by a network 112 having a multi-casting function. The update values of more than one update **data** belonging to the same parity **group** and the set of values before update are broadcast to the disk device 105. The respective disk devices 105 accumulate the update value of received update **data** and the values before update in a buffer 109, execute scheduling by considering seeking/searching **item** and decide a processing **order** . The disk device storing a parity takes out the update value of update **data** and the value before update from the **buffer** in order, reads the value of the parity before update, generates the update value and writes it into the disk 110. The disk device storing data takes out the update value of update **data** from the **buffer** 109 in **order** and writes it into a disk 110. Thus, the throughput of the system 1 can be improved.

29/5/9 (Item 9 from file: 347)

DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

04212855 **Image available**
MULTIPLE DISK DEVICE

PUB. NO.: 05-204555 [JP 5204555 A]
PUBLISHED: August 13, 1993 (19930813)
INVENTOR(s): ONO TOSHIIE
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-011173 [JP 9211173]
FILED: January 24, 1992 (19920124)
INTL CLASS: [5] G06F-003/06
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units); 42.5 (ELECTRONICS -- Equipment)
JOURNAL: Section: P, Section No. 1649, Vol. 17, No. 634, Pg. 31, November 24, 1993 (19931124)

ABSTRACT

PURPOSE: To shorten the processing time by multiplexing input/output **requests** to individual **disk** devices.

CONSTITUTION: This system is characterized by providing a **disk drive** which enqueues an input **request** to a **disk** device **group** in input/output **request queues** 4 of all **disk** devices constituting the group and updates a preceding device number 2 of a controller management block 1 with the next device number of rotation to enqueue an output **request** in the input/output **request queue** of the **disk** device having this device number. At the time of execution of the input/output **request** , this **disk drive** takes out one input/output **request** from the input/output **request queue** of each **disk** device and simultaneously **requests** a **disk** controller to seek respective **disk** devices and individually **requests data** read/write in the reception **order** of seek completion interrupts.

29/5/10 (Item 10 from file: 347)

DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

04186176 **Image available**
TAPE PRINTER

PUB. NO.: 05-177876 [JP 5177876 A]

PUBLISHED: July 20, 1993 (19930720)
INVENTOR(s): UENO HIDEO
SAKURAGI SHOJI
NIWA AKIHIKO
APPLICANT(s): BROTHER IND LTD [000526] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-358987 [JP 91358987]
FILED: December 26, 1991 (19911226)
INTL CLASS: [5] B41J-002/485; B41J-003/407; B41J-003/46; G06F-003/12
JAPIO CLASS: 29.4 (PRECISION INSTRUMENTS -- Business Machines); 45.3 (INFORMATION PROCESSING -- Input Output Units)
JAPIO KEYWORD: R011 (LIQUID CRYSTALS); R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: M, Section No. 1503, Vol. 17, No. 595, Pg. 154, October 29, 1993 (19931029)

ABSTRACT

PURPOSE: To **obtain** a **tape** printer which can perform a partial emphasis by framing to conduct printing with various impression.

CONSTITUTION: When a printing key is operated after the input of required data, data is read out of a character storage area. If the **data** is character data (S45: No), printing **pattern data** is **arranged** in an image **buffer** (S46). If the **data** is partially framing **data** (S45: Yes), a vertical line printing **pattern** for a partial framing is arranged in the image **buffer** . When all the **data** in the character storage area are read out, a horizontal line printing pattern for a partial framing is arranged (S50). After that, a printing pattern for a total framing is arranged in the image buffer (S52). A printing action is executed based on the printing pattern in the image buffer (S53).

29/5/11 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

04036380 **Image available**
INPUT/OUTPUT CONTROLLER

PUB. NO.: 05-028080 [JP 5028080 A]
PUBLISHED: February 05, 1993 (19930205)
INVENTOR(s): WATANABE FUMIO
APPLICANT(s): NEC IBARAKI LTD [490946] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-182654 [JP 91182654]
FILED: July 23, 1991 (19910723)
INTL CLASS: [5] G06F-013/12
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 1555, Vol. 17, No. 308, Pg. 148, June 11, 1993 (19930611)

ABSTRACT

PURPOSE: To improve the processing efficiency by writing data, which is transferred by plural transfer requests from a channel which does not report the final transfer of a **series** of **data** transfer at the time of input transfer, in a main **storage** by one transfer **request** .

CONSTITUTION: A channel priority discriminating circuit 30 which selects firmware interrupt **requests** from plural channels, an input **data buffer** 40 where plural transfer **data** are stored, a processor part 70, an input transfer control part 50, etc., are provided. At the time of the lower-order end of input transfer to the channel which does not report the final transfer of a **series** of **data** transfer, the processor part 70 outputs a final transfer instruction to an input transfer control circuit 50 by the firmware interrupt request from the same channel. Then, the input transfer control circuit 50 **requests** write to the main **storage** , and data which is not written in the main storage at the time of the lower-**order** end is transferred. Consequently, transfer **data** to plural transfer requests from the channel are transferred by one **request** of

transfer to the main **storage** .

29/5/13 (Item 13 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

03292121 **Image available**
I/O PRIORITY DECIDING SYSTEM FOR COMPUTER

PUB. NO.: 02-267621 [JP 2267621 A]
PUBLISHED: November 01, 1990 (19901101)
INVENTOR(s): OGAWA KENJI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-088601 [JP 8988601]
FILED: April 07, 1989 (19890407)
INTL CLASS: [5] G06F-003/14
JAPIO CLASS: 45.3 (INFORMATION PROCESSING -- Input Output Units)
JOURNAL: Section: P, Section No. 1156, Vol. 15, No. 24, Pg. 14, January 21, 1991 (19910121)

ABSTRACT

PURPOSE: To increase the processing speed of the window desired by a user by scheduling with preference the I/O process of an upper window.

CONSTITUTION: If an instruction is received so as to set a window B, for example, at the highest place, the superposition **information** is set in **order** of windows B, C and A. A priority switch instruction means 8 gives an instruction to an I/O driver 10 to give the highest priority to the I/O corresponding to the window B. The **driver** 10 **queues** the I/O **request** received from a process **group** 9 and connects again the I/O **request** of the window B designated by the means 8 to the head of the queue. Therefore the I/O requested from the highest window B is processed earliest among those I/O requests given to a peripheral device 12. As a result, the processing speed is increased for the window desired by a user.

29/5/16 (Item 16 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

02838663 **Image available**
SYSTEM FOR MANAGING COMMUNICATION CONTROL BUFFER

PUB. NO.: 01-136263 [JP 1136263 A]
PUBLISHED: May 29, 1989 (19890529)
INVENTOR(s): ITO AKINORI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-297078 [JP 87297078]
FILED: November 24, 1987 (19871124)
INTL CLASS: [4] G06F-013/00
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 925, Vol. 13, No. 389, Pg. 18, August 29, 1989 (19890829)

ABSTRACT

PURPOSE: To use a common **buffer** area without lowering processing efficiency in **data** transfer by performing the data transfer between layers by transferring the managing right of the **buffer** area as leaving **data** stored in the **buffer** area as it is.
CONSTITUTION: In transmission, a communication control program of high-**order** layer starts up a **data** generating means 19 to perform the transmission. The **data** generating means 19 **requests** the **buffer** area to a **buffer** acquiring means 12. The buffer acquiring means 12 searches a null **buffer** from a buffer area **group** . The **data** generating means 19 stores transmission **data** in the **data** **storage** area 22 of the **buffer** ,

and **requests** **data** transmission to a low- **order** transmission means 16. The transmission means 16 informs the **buffer** are where the transmission **data** is stored to a low- **order** layer. The communication control program of low- **order** , when accepting a transfer **request** from the high- **order** layer by a high- **order** acceptance means 15, **requests** the re-acquirement of the **buffer** to a buffer re-acquiring means 13.

29/5/18 (Item 18 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

02328564 **Image available**
DMA CONTROLLER FOR ELECTRONIC COMPUTER SYSTEM

PUB. NO.: 62-245464 [JP 62245464 A]
PUBLISHED: October 26, 1987 (19871026)
INVENTOR(s): SUZUKI TAKASHI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-089611 [JP 8689611]
FILED: April 18, 1986 (19860418)
INTL CLASS: [4] G06F-013/28
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD:R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: P, Section No. 689, Vol. 12, No. 119, Pg. 69, April 14, 1988 (19880414)

ABSTRACT

PURPOSE: To reduce the **load** on the **rearrangement** of **data** structure in a main **storage** device by a central processing unit by bringing an address generating circuit in a DMA controller under programmed control corresponding to the data structure in the main storage device.

CONSTITUTION: An input/output **instruction** **buffer** 22a, a signal line 23, an **address** register 24, a microprocessor 25, a signal line 27, an address table 29, and a signal line 31 constitute an **address** **pattern** generating circuit. When the microprocessor 25 receives a **request** for data transfer from the main **storage** device 12 and data structure information on the main storage device through the signal line 23, an address to be accessed in the main storage device 12 is calculated based on the values and written on the address table 29 composed of a RAM through the signal line 27. Only necessary part in the **data** structure **arranged** in the main **storage** device is accessed to reduce the **load** on the rearrangement of the main **storage** device by the central processing unit.

29/5/20 (Item 20 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

01966232 **Image available**
DATA **STORAGE** AND **RETRIEVAL** SYSTEM

PUB. NO.: 61-180332 [JP 61180332 A]
PUBLISHED: August 13, 1986 (19860813)
INVENTOR(s): KONDO HIDEFUMI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-019937 [JP 8519937]
FILED: February 06, 1985 (19850206)
INTL CLASS: [4] G06F-007/28
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic **Sequence** Units); 45.2 (**INFORMATION** PROCESSING -- Memory Units
JOURNAL: Section: P, Section No. 532, Vol. 11, No. 2, Pg. 96, January 06, 1987 (19870106)

ABSTRACT

PURPOSE: To increase the storage amount of data related to the same block and to attain the retrieval at a high speed in a retrieval mode by designating the number of correspondences between related data before storage of data through a table.

CONSTITUTION: This system comprises an external memory 201, a card reader 202, a terminal equipment 203, a channel 204, a CPU205 and a main memory 206. The memory 206 contains a **data** base control system DBMS207 and a **buffer** area 208. When an inter-table **data** ratio (inter-table correspondence number) is given to the DBMS207 from the equipment 203, the DBMS207 **arranges** the received **data** in the area 208 according to a storage type stored in the memory 201 and transfers them to the memory 201 for writing. When the storage is through with the inter-table data ratio, the DBMS207 decides a storage section for each table with a data storage block.

29/5/24 (Item 24 from file: 347)

DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

01848834 **Image available**

CONTROL METHOD OF INFORMATION RETRIEVAL

PUB. NO.: 61-062934 [JP 61062934 A]
PUBLISHED: March 31, 1986 (19860331)
INVENTOR(s): HOSHINO MASAYUKI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-184601 [JP 84184601]
FILED: September 05, 1984 (19840905)
INTL CLASS: [4] G06F-007/28
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic **Sequence** Units); 45.2 (**INFORMATION** PROCESSING -- Memory Units
JOURNAL: Section: P, Section No. 485, Vol. 10, No. 229, Pg. 68, August 08, 1986 (19860808)

ABSTRACT

PURPOSE: To obtain retrieved information based upon invariably up-to-date **information** by accessing a **buffer** memory by a central processor by performing retrieval automatically after information writing operation and storing the retrieval result in the buffer memory previously.

CONSTITUTION: When an instruction decoded by an instruction decoding part 1 is a retrieval instruction, the retrieval **instruction** is stored in a retrieval **instruction queue buffer** 3 and an indication of retrieval operation is sent to a retrieval control part 4. The **retrieval** control part 4 reads data out of an external **storage** device and stores the **retrieval** result in the buffer 6 in order according to the **queue order** in the **instruction** retrieval **queue buffer** 3. Then, when a retrieval result readout **instruction** is supplied from a central processor, the contents of the buffer 6 are sent out to the central processor. The retrieval result information based upon up-to-date information in the external **storage** device is acquired automatically in the **buffer** in an **information retrieving** device without the intervention of a program, so a program uses the retrieval result at a high speed.

29/5/25 (Item 25 from file: 347)

DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

01747438 **Image available**

INFORMATION RETRIEVING SYSTEM

PUB. NO.: 60-225938 [JP 60225938 A]
PUBLISHED: November 11, 1985 (19851111)

INVENTOR(s): TAKEDA HARUO
TABATA KUNIAKI
NAKAMURA MASAO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-081759 [JP 8481759]
FILED: April 25, 1984 (19840425)
INTL CLASS: [4] G06F-007/28
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic **Sequence** Units); 45.2 (**INFORMATION** PROCESSING -- Memory Units
JOURNAL: Section: P, Section No. 444, Vol. 10, No. 89, Pg. 156, April 08, 1986 (19860408)

ABSTRACT

PURPOSE: To execute a retrieval at a high speed by providing separately a recording device which can erase and rewrite, together with an optical disk device, **sorting** an index part of a **data** and storing it in this recording device, when installing an optical disk.

CONSTITUTION: When registering a document picture data, an original document from a scanner is stored in an optical disk 16 by using a picture memory 13 as a **buffer** , by adding additional **information** such as a key word, etc. inputted from a keyboard 14. In this state, when installing an optical disk, a signal of an installing completion from the optical disk 16 is received by a CPU11, and based on the signal, the CPU11 reads out an index part of the optical disk 16 to a memory 12, executes the sort processing, and thereafter, stores this result in a magnetic **disk** 17. Also, when executing a **retrieval** , an index coinciding with a key word inputted from the magnetic disk 17 is searched by a command from the keyboard 14. Subsequently, based on address information of the optical disk in the searched index information, a document picture data are read out to the picture memory 13 from the optical disk 16, and they are displayed on a display 18.

29/5/26 (Item 26 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

01466964 **Image available**
DYNAMIC CHANGING SYSTEM OF ACCESS PRIORITY ORDER

PUB. NO.: 59-178564 [JP 59178564 A]
PUBLISHED: October 09, 1984 (19841009)
INVENTOR(s): KITAZAWA MASAHIRO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-054193 [JP 8354193]
FILED: March 30, 1983 (19830330)
INTL CLASS: [3] G06F-013/00; G06F-009/46; G06F-015/16; G11C-009/06
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.1 (INFORMATION PROCESSING -- Arithmetic **Sequence** Units); 45.4 (**INFORMATION** PROCESSING -- Computer Applications
JOURNAL: Section: P, Section No. 335, Vol. 09, No. 37, Pg. 98, February 16, 1985 (19850216)

ABSTRACT

PURPOSE: To enable dynamic change of already set priority **order** according to the state of **data** storing of accessed part by providing a circuit that detects inability of taking out data from accessed section more than specified number of times in a specified time.

CONSTITUTION: Every time access **request** is made to a main **storage** , number of times of access **request** is counted up by 1 by a detecting circuit 1. When the number of times arrives at a specified number of times in a specified time, an output signal is generated from the circuit 1 and supplied to a priority order determining circuit 2. By this, priority order is dynamically changed so that right of access is given to access **request**

of next priority **order** instead of giving right of access to a **buffer storage** (a) to access **request** of competing highest priority **order** . Thus, capacity of the system can be improved without generating overrun in a channel.

29/5/27 (Item 27 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

01037428 **Image available**
DATA TRANSFER CONTROL METHOD

PUB. NO.: 57-187728 [JP 57187728 A]
PUBLISHED: November 18, 1982 (19821118)
INVENTOR(s): FUJITA MITSUAKI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-072807 [JP 8172807]
FILED: May 14, 1981 (19810514)
INTL CLASS: [3] G06F-003/00; G06F-005/06; G06F-013/00
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic **Sequence** Units); 45.2 (**INFORMATION** PROCESSING -- Memory Units
JOURNAL: Section: P, Section No. 175, Vol. 07, No. 35, Pg. 66, February 10, 1983 (19830210)

ABSTRACT

PURPOSE: To **arrange** and store **data** in a **buffer** storage device of the **data request** source in the **order** of **data request** even if **data** is transferred in the **order** different from the **order** of **data request** , by providing a means for transmission of signals which indicate **storage** addresses in the data **request** source.

CONSTITUTION: When a request start signal 21 is outputted from an operation controlling circuit 2, a request controlling circuit 3 is started, and contents of a **buffer address** counter 13 are updated. A **data request** signal 8 is sent from the **request** controlling circuit 3 to **storage** devices 5-7 in the **order** of RQ1-RQ3, and an **address** signal is sent from an **address** register 4 in the **order** of AD1- AD3 to indicate **addresses** in **storage** devices where **requested** information should be stored. After the **storage** device 5 finds that the address AD1 for RQ1 is in the storage device 5 itself, the storage device 5 starts the access operation to AD1 and stores contents N of an output signal 22 of the **buffer address** counter 13 in a **data** storage **address** register 51 and transmits contents N when information DT1 is outputted.

29/5/28 (Item 28 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

00958772 **Image available**
DATA RETRIEVAL SYSTEM

PUB. NO.: 57-109072 [JP 57109072 A]
PUBLISHED: July 07, 1982 (19820707)
INVENTOR(s): OKAJIMA HIDENOBU
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-186813 [JP 80186813]
FILED: December 26, 1980 (19801226)
INTL CLASS: [3] G06F-013/04; G06F-007/28; G06F-015/40
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.1 (INFORMATION PROCESSING -- Arithmetic **Sequence** Units); 45.4 (**INFORMATION** PROCESSING -- Computer Applications
JOURNAL: Section: P, Section No. 148, Vol. 06, No. 203, Pg. 21, October 14, 1982 (19821014)

ABSTRACT

PURPOSE: To speed processing by decreasing the frequency of access to an external **storage** device for **retrieval** , by making respective keys different in **arrangement** of position **information** by preparing a set of pieces of position information on an element and its preceding element of a chain in the external storage device for each key.

CONSTITUTION: To find chains that keys 1 and 2 of a data **storage** address **request** origin 50 have among chains 12-17 among data elements in an external **storage** device 40, values **obtained** from the keys 1 and 2 by hash tecnique and the values of pointer registers 3 and 4 to control tables 8 and 9 provided for respective attributes are applied to arithmetic circuits 21 and 22 which calculate a stacker starting address to be processed. Then, **pointer** values to stacker **buffers** 10 and 11 stored with element storage **addresses** having the same key in tables 8 and 9 are stored are obtained in starting- **address** registers 5 and 6 in the **buffers** . A **pointer** to an element which has keys 1 and 2 of the buffers 10 and 11 is searched by a comparing circuit 23 to inform a request origin of an element pointed in common.

29/5/29 (Item 29 from file: 347)

DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

00919037 **Image available**
DATA BASE ACCESS SYSTEM

PUB. NO.: 57-069337 [JP 57069337 A]
PUBLISHED: April 28, 1982 (19820428)
INVENTOR(s): KIMIJIMA HIROAKI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-141621 [JP 80141621]
FILED: October 09, 1980 (19801009)
INTL CLASS: [3] G06F-007/22; G06F-003/04
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic **Sequence** Units); 45.2 (**INFORMATION** PROCESSING -- Memory Units); 45.3 (INFORMATION PROCESSING -- Input Output Units
JOURNAL: Section: P, Section No. 133, Vol. 06, No. 148, Pg. 111, August 07, 1982 (19820807)

ABSTRACT

PURPOSE: To effectively use the process of plural terminals at the **request** side through an image copying part, by providing a buffer **storage** part to store the process conditions corresponding to each terminal and originating a data base access instruction through the image copying part to an access control part by the said process conditions.

CONSTITUTION: When an access instruction of other system is originated through plural terminal devices TERM1-n, a communication control part CCP in a data base process means CPD of a center receives the **data** . The **queue** is produced at this part CCP for the transmitted microinstruction and then sent to an image copying part DIM one by one in the **order** of the wait **request** . At the same time, the control **data** of each terminal is produced to **buffer** storage parts BUF1-n at a **buffer** control part DMC in a **data** base control part DBC in correspondence to the microinstruction given from devices TERC1-n. Then the using buffer numbers corresponding to the devices TERM1-n are sent to the part DIM.

29/5/30 (Item 30 from file: 347)

DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

00603449 **Image available**
FILE ACCESS CONTROL SYSTEM

PUB. NO.: 55-091049 [JP 55091049 A]
PUBLISHED: July 10, 1980 (19800710)
INVENTOR(s): KURIMURA SHINICHIRO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 53-162385 [JP 78162385]
FILED: December 29, 1978 (19781229)
INTL CLASS: [3] G06F-013/04; G11B-005/09
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 42.5 (ELECTRONICS -- Equipment)
JOURNAL: Section: P, Section No. 30, Vol. 04, No. 142, Pg. 99, October 07, 1980 (19801007)

ABSTRACT

PURPOSE: To secure the highly efficient process for the I/O **requests** to the magnetic **disk** by rearranging a **series** of I/O **requests** in the **order** of the cylinder **addresses** at the side of the file subsystem and then giving execution to the input/output process **requests** also in the **order** of the cylinder **addresses** .

CONSTITUTION: A pair of buffers 6-A and 6-B are provided in correspondence to each subchannel. And the I/O requests given from the central process unit are stacked in the order of input to either one of the buffer pair such as buffer 6-A which is under WAIT state, and then the input to buffer 6-A is stopped at an optional time. Then the I/O **requests** within **buffer** 6-A are **rearranged** in the rising **order** of the cylinder **addresses** via **sorting** circuit 7, and the I/O **requests** are processed in **sequence** . After stopping the input to **buffer** 6-A, the I/O **requests** are stacked to **buffer** 6-B along with the rearrangement and processing given in the same way. These actions are repeated in the alternate way to perform the scan scheduling, thus reducing the seeking time greatly.

29/5/31 (Item 1 from file: 350)

DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

016754411 **Image available**
WPI Acc No: 2005-078689/200509
XRPX Acc No: N05-069071

Input/output request **executing method for hard** disk drive , **involves determining** ordering **of input/output** requests **according to adjusted delay times, and executing I/O** request **according to determined** ordering

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: LAMBERTS B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040255055	A1	20041216	US 2003463012	A	20030616	200509	B

Priority Applications (No Type Date): US 2003463012 A 20030616
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040255055	A1		12	G06F-003/00	

Abstract (Basic): US 20040255055 A1

NOVELTY - The method involves determining delay times associated with processing a **group** of input/output (I/O) **requests** . The determined delay times for the I/O requests are adjusted according to priorities assigned to the I/O **requests** . An **ordering** of the I/O **requests** is determined according to the adjusted delay times. An I/O request is executed according to the determined ordering.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(A) a system for executing I/O requests

(B) an article of manufacture for executing I/O requests.

USE - Used for executing an input/output (I/O) **request** for a hard

disk drive .

ADVANTAGE - The method efficiently executes the I/O **requests** for **reordering** the I/O **queues** , so that response times for the **requests** are optimized.

DESCRIPTION OF DRAWING(S) - The drawing shows a diagram of a hard disk drive unit.

Disk drive system (2)
Rotating disks (4)
Actuator assembly (6)
Slider (8)
Current driver (10)
pp; 12 DwgNo 2/5

Title Terms: INPUT; OUTPUT; REQUEST; EXECUTE; METHOD; HARD; DISC; DRIVE; DETERMINE; ORDER; INPUT; OUTPUT; REQUEST; ACCORD; ADJUST; DELAY; TIME; EXECUTE; REQUEST; ACCORD; DETERMINE; ORDER
Derwent Class: T01; T03
International Patent Class (Main): G06F-003/00
File Segment: EPI

29/5/33 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

014414845 **Image available**
WPI Acc No: 2002-235548/200229
Related WPI Acc No: 1998-362235; 2000-223426
XRPX Acc No: N02-180875

Instruction reordering buffer **system for computer processors using a Last in** buffer **indicator to indicate** instruction **position and operand dependency**

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: TRAN T M; WITT D B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6292884	B1	20010918	US 97803093	A	19970220	200229	B
			US 9878213	A	19980513		
			US 99476388	A	19991230		

Priority Applications (No Type Date): US 97803093 A 19970220; US 9878213 A 19980513; US 99476388 A 19991230
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6292884	B1		31	G06F-009/30	Cont of application US 97803093
					Cont of application US 9878213
					Cont of patent US 5768555
					Cont of patent US 6032251

Abstract (Basic): US 6292884 B1

NOVELTY - The destination operand specifiers are **loaded** into the **instruction storage buffer** (80) and the Last In **Buffer** (LIB) indication added. During execution of **instructions** , the LIB indicator is also used to indicate operand dependency, allowing independent operand instructions to be extracted by the dependency checking unit (82) for concurrent execution.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a computer system and a method of operating a reorder buffer within a microprocessor.

USE - To **order instructions** execution **sequences** within a microprocessor allowing concurrent execution.

ADVANTAGE - By including the Last In Buffer indicator within the reordering buffer, the indicator can also be used to indicate operand dependency between **instructions** removing the need for additional **prioritization** logic. Thus reducing the comparison delay improves execution speed.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of the reordering buffer.

instruction storage **buffer** (80)
dependency checking unit (82)
pp; 31 DwgNo 4/10
Title Terms: INSTRUCTION; BUFFER; SYSTEM; COMPUTER; PROCESSOR; LAST; BUFFER ; INDICATE; INDICATE; INSTRUCTION; POSITION; OPERAND; DEPEND
Derwent Class: T01; U14; U21
International Patent Class (Main): G06F-009/30
File Segment: EPI

29/5/34 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

013457558 **Image available**
WPI Acc No: 2000-629501/200061
XRPX Acc No: N00-466520
Memory access request handling unit e.g. between processor and cache for data processing system by re- ordering **the** sequence **after comparison of access** requests **in** queue
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: HARRIS J G
Number of Countries: 028 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1026594	A2	20000809	EP 2000300820	A	20000202	200061	B
CA 2298242	A1	20000808	CA 2298242	A	20000208	200061	
JP 2000242545	A	20000908	JP 200030533	A	20000208	200061	
US 6601151	B1	20030729	US 99246614	A	19990208	200354	

Priority Applications (No Type Date): US 99246614 A 19990208
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1026594	A2	E	17	G06F-013/16	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
CA 2298242	A1	E		G06F-013/16	
JP 2000242545	A		13	G06F-012/00	
US 6601151	B1			G06F-013/16	

Abstract (Basic): EP 1026594 A2
NOVELTY - The transmission unit (40) is arranged to monitor a window (34) of the queue (30). The comparator (45) selects one or more of the **queue** elements (32) based on memory access **requests** not yet transmitted to the data **storage** element (20).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of handling memory access requests in a data processing system.
USE - For data processing system.
ADVANTAGE - The throughput of memory access requests is increased independent of access times and memory bandwidth.
DESCRIPTION OF DRAWING(S) - The figure shows a schematic block diagram of a memory access request handling unit.
Storage Elements (20)
Queue (30)
Queue Elements (32)
Window (34)
Transmission Unit (40)
Comparator (45)
pp; 17 DwgNo 1/10
Title Terms: MEMORY; ACCESS; REQUEST; HANDLE; UNIT; PROCESSOR; CACHE; DATA; PROCESS; SYSTEM; ORDER; SEQUENCE; AFTER; COMPARE; ACCESS; REQUEST; QUEUE
Derwent Class: T01
International Patent Class (Main): G06F-012/00; G06F-013/16
International Patent Class (Additional): G06F-012/08; G06F-013/18
File Segment: EPI

29/5/35 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

013455194 **Image available**
WPI Acc No: 2000-627137/200060
XRPX Acc No: N00-464661
Method and device for servicing requests of computer system users (options)
Patent Assignee: MILITARY COMMUNIC ACAD (MILI-R)
Inventor: ALDUKHOV A A; BUSHUEV S N; PASHCHENKO V V; PEREVYAZKIN A V; ZHILYAKOV A I
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
RU 2140666	C1	19991027	RU 98113202	A	19980706	200060	B

Priority Applications (No Type Date): RU 98113202 A 19980706
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
RU 2140666	C1			G06F-009/46	

Abstract (Basic): RU 2140666 C1
NOVELTY - Method involves generation of maximum **request** -waiting time codes, their storage, shaping of **request** servicing signals, **organization** of second- **order** **queue** of arriving **requests** according to user's priority number, transfer of second- **order** **requests** to first-order **queue** in **sequence** in which their maximum wait time ((tmi)) in second-order **queue** is out, servicing of first- **order** **requests** and, if they are not available, doing so with second- **order** **requests** . Each device has N similar user's units, clock generator, divider, NOR gate, counter, AND gate, inverter, and multiplexer.
USE - Computer engineering; data exchange systems.
ADVANTAGE - Improved probability of servicing low-priority requests in due time. 5 cl, 6 dwg
pp; 0 DwgNo 1/1
Title Terms: METHOD; DEVICE; SERVICE; REQUEST; COMPUTER; SYSTEM; USER; OPTION
Derwent Class: T01; U21
International Patent Class (Main): G06F-009/46
File Segment: EPI

29/5/37 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

012711782 **Image available**
WPI Acc No: 1999-517895/199943
XRPX Acc No: N99-385136
Queued **memory** requests **flushing system**
Patent Assignee: COMPAQ COMPUTER CORP (COPQ)
Inventor: FOSTER J E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5948081	A	19990907	US 97995367	A	19971222	199943	B

Priority Applications (No Type Date): US 97995367 A 19971222
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5948081	A		11	G06F-007/00	

Abstract (Basic): US 5948081 A
NOVELTY - A memory controller (38) flushes any previous memory **requests** to a memory before servicing a current memory **request** . **Storage** locations are **ordered** from top (52b) to bottom (50a) of **request** **queue** (46). A **request** **queue** (44) includes a counter

associated with current **request queue** with location value of previous memory **request** relative to top of initial **queue** .

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a memory **request series** bursting method.

USE - For flushing **queued** memory read and write **requests** and all prior write requests with a counter indicating requests to be flushed in computer systems.

ADVANTAGE - By **arranging** the memory write **request** optimally the memory bus bandwidth can be improved. The corruption of read and write requests can be prevented by queuing the request and cross snooping between the requests.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of a memory queue memory.

Memory controller (38)

Request queue (46,44)

Bottom location of queue (50a)

Top location queue (52b)

Queue controller (58)

pp; 11 DwgNo 3/4

Title Terms: QUEUE; MEMORY; REQUEST; FLUSH; SYSTEM
Derwent Class: T01
International Patent Class (Main): G06F-007/00
File Segment: EPI

29/5/39 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

012587946 **Image available**
WPI Acc No: 1999-394053/199933
XRPX Acc No: N99-294476

Quantitative operational analysis method of I/O devices such as direct access storage device

Patent Assignee: EMC CORP (EMCE-N)
Inventor: LECRONE D E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5913073	A	19990615	US 97948752	A	19971010	199933	B

Priority Applications (No Type Date): US 97948752 A 19971010
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5913073	A		26	G06F-011/30	

Abstract (Basic): US 5913073 A

NOVELTY - A pseudo operating system is initialized to generate **ordered sequence** of I/O **requests** to a specific device, in response to a benchmark initialization command. A request object is then created and transferred to the dispatcher queue by selectively activating driver to enable transfer to designated I/O device via the mark operating system, responding to each I/O request.

DETAILED DESCRIPTION - The pseudo operating system has a pool of machine drivers, machine request objects pool, device tables pool and a dispatcher **queue** . The **request** object is created in response to an I/O **request** . The selected inactive **driver** is activated for performing the transfer. The number of drivers depends on the number of central processors and not on the number of devices. The benchmark is finally terminated in response to another command and the active drivers are inactivated to be available for other actions. An INDEPENDENT CLAIM is also included for the system for testing the operation of data processing system.

USE - For operation of I/O devices such as direct access devices (DASD) used in large in data processing system.

ADVANTAGE - Improves operation of I/O devices by minimizing the overhead imposed by benchmark tests. Provides accurate quantitative performance evaluation at high I/O rates of large numbers of I/O

devices.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the data processing system using the benchmark method.
pp; 26 DwgNo 1/12
Title Terms: QUANTITATIVE; OPERATE; ANALYSE; METHOD; DEVICE; DIRECT; ACCESS ; STORAGE; DEVICE
Derwent Class: T01
International Patent Class (Main): G06F-011/30
File Segment: EPI

29/5/42 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

011074614 **Image available**
WPI Acc No: 1997-052538/199705
XRPX Acc No: N97-043036
Processing method for multiple requests **and out of** order **returns - involves converting CPU requests into cache control** requests **, such that** sequence **of multiple** requests **for** data **can be sent to low level** storage **devices or shared buses**
Patent Assignee: SEIKO EPSON CORP (SHIH); S-MOS SYSTEMS INC (SMOS-N)
Inventor: HAGIWARA Y; NGUYEN L T
Number of Countries: 020 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9641250	A2	19961219	WO 96US8549	A	19960603	199705	B
WO 9641250	A3	19970306	WO 96US8549	A	19960603	199728	
US 5778434	A	19980707	US 95479035	A	19950607	199834	
US 6173369	B1	20010109	US 95479035	A	19950607	200104	
			US 9824134	A	19980217		

Priority Applications (No Type Date): US 95479035 A 19950607; US 9824134 A 19980217
Cited Patents: No-SR.Pub; EP 292188; EP 568231; US 4370710
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9641250	A2	E	44	G06F-000/00	
Designated States (National): JP KR					
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
WO 9641250	A3			G06F-000/00	
US 5778434	A			G06F-012/00	
US 6173369	B1			G06F-013/00	Cont of application US 95479035 Cont of patent US 5778434

Abstract (Basic): WO 9641250 A
The method involves processing a **sequence** of **requests** for **data** by one or more CPUs after cache misses. Each CPU request includes a CPU-ID tag identifying the CPU issuing the request for data, and an address identifying a location in lower-level memory where the data is stored. Cache control ID tags are assigned to identify the locations in the **request queue** of the respective CPU-ID tags associated with each CPU request.
Cache-control requests consisting of the cache-control ID tags and the respective **address** information, are sent from the **request queue** to the lower-level memory or **storage** devices. Data is then returned together with the corresponding CPU-ID tags in the order in which it is returned by the **storage** devices. The **sequence** of CPU **requests** for **data** is fulfilled by returning the data and the CPU-ID tag in the **order** in which the **data** was returned from memory.
ADVANTAGE - Data is retrieved after cache misses more quickly and efficiently than processing **data requests** in **sequence** . Cache control ID tags allow individual **requests** to be distinguished such that multiple requests for data can be pending at same time.
Dwg.1/11
Title Terms: PROCESS; METHOD; MULTIPLE; REQUEST; ORDER; RETURN; CONVERT;

CPU; REQUEST; CACHE; CONTROL; REQUEST; SEQUENCE; MULTIPLE; REQUEST; DATA; CAN; SEND; LOW; LEVEL; STORAGE; DEVICE; SHARE; BUS
Derwent Class: T01
International Patent Class (Main): G06F-000/00; G06F-012/00; G06F-013/00
International Patent Class (Additional): G06F-000/00; AFG0-6F012/00; AG-G06F013/00
File Segment: EPI

29/5/45 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

009848662 **Image available**
WPI Acc No: 1994-128518/199416
XRPX Acc No: N94-100944
Image processing system for video editing or compositing - transfers groups of data to video tape for storage so that data for each sub-image can be retrieved independently from data for other sub-images
Patent Assignee: QUANTEL LTD (QUAO)
Inventor: HINSON N R; KELLAR P R N; NONWEILER B R G
Number of Countries: 006 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2272126	A	19940504	GB 9222658	A	19921028	199416	B
EP 595556	A1	19940504	EP 93308412	A	19931022	199418	
JP 6225261	A	19940812	JP 93269005	A	19931027	199437	

Priority Applications (No Type Date): GB 9222658 A 19921028
Cited Patents: GB 2179819; GB 2231463; GB 2238214; US 4984286; WO 9107061
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2272126	A		32	H04N-007/12	
EP 595556	A1	E	11	H04N-005/92	
Designated States (Regional): DE FR GB IT NL					
JP 6225261	A		9	H04N-005/92	

Abstract (Basic): GB 2272126 A
The image processing system (1) comprises frame stores (3,4) and a disc store (6) connected via a **buffer** (1), all controlled by a processor (12). **Data** , representing an image at high resolution, are moved between the stores in **order** to create sets of **data** representing respective sub-images. Each sub-image represents the entire image but at a lower resolution.
The sub-image data are recorded on video tape by a recorder (17). This enables the sub-image data to be transferred to low resolution processing appts. for processing and/or display of the sub-images. Processed low resolution sub-images may be represented to give a high resolution image.
Dwg.1/4
Title Terms: IMAGE; PROCESS; SYSTEM; VIDEO; EDIT; COMPOSITOR; TRANSFER; GROUP; DATA; VIDEO; TAPE; STORAGE; SO; DATA; SUB; IMAGE; CAN; RETRIEVAL; INDEPENDENT; DATA; SUB; IMAGE
Derwent Class: W04
International Patent Class (Main): H04N-005/92; H04N-007/12
International Patent Class (Additional): G06F-015/62; H04N-005/262; H04N-005/907
File Segment: EPI

29/5/46 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

009578736 **Image available**
WPI Acc No: 1993-272282/199334
XRPX Acc No: N93-209144
Integrated thin film electrographic writing head for recording upon

medium - has marking electrodes arranged in linear array for writing data onto medium with selector supplying signal to buffer for data loading

Patent Assignee: XEROX CORP (XERO)
Inventor: DA COSTA V M; OCONNELL P A
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5237346	A	19930817	US 92871250	A	19920420	199334	B
JP 6040068	A	19940215	JP 9376804	A	19930402	199411	
JP 3351847	B2	20021203	JP 9376804	A	19930402	200281	

Priority Applications (No Type Date): US 92871250 A 19920420
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5237346	A		14	G01D-015/06	
JP 6040068	A			B41J-002/385	
JP 3351847	B2		11	B41J-002/385	Previous Publ. patent JP 6040068

Abstract (Basic): US 5237346 A

The writing head has integrated marking electrodes or bits (12) arranged in a linear array for writing onto a medium, and a plurality of high voltage driving circuits (90) for driving the nibs. The write head also includes a plurality of latches (80) each connected to the high voltage driving circuits, a plurality of memory cells (70) each connected to the latches, a plurality of buffers (60), each buffer supplying a select line to the plurality of memory cells, and a plurality of selection elements, supplying a selection signal to each of the buffers to drive a segment of memory cells. The integrated memory and latch circuits allow for simultaneous latching and writing of an entire scanline of data.

During operation, write input Vw is set low, disconnecting the HV driving circuit from output of RAM cell, and will remain in its last state. Next, all RAM cells on head are set low by pulsing present signal Vps high; a low logic is shifted down dynamic shift register (50) which is buffered (70) at the output sequentially enabling the select line VG; - this selects each group of thirty-two RAM cells in turn. Once all RAM cells **group** are loaded (on head) with **data** (entire scanline of data) write signal Vw is set to a logic high and RAM cells outputs are simultaneously latched, switching nib potentials for writing.

ADVANTAGE - Control of writing Vw pulses separately for each section allows data from each section to be written onto medium, to look as if each section was physically aligned and all the data in a scanline were written simultaneously. Capable of accessing separate segments on head randomly.

Dwg.2/8

Title Terms: INTEGRATE; THIN; FILM; ELECTROGRAPH; WRITING; HEAD; RECORD; MEDIUM; MARK; ELECTRODE; ARRANGE; LINEAR; ARRAY; WRITING; DATA; MEDIUM; SELECT; SUPPLY; SIGNAL; BUFFER; DATA; LOAD
Derwent Class: P75; T04; U14
International Patent Class (Main): B41J-002/385; G01D-015/06
International Patent Class (Additional): H04N-001/032
File Segment: EPI; EngPI

29/5/64 (Item 34 from file: 350)

DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

003319051
WPI Acc No: 1982-G7065E/198223

Electronic digital processor for real time text processing - includes arrangement scheduling execution of instruction sequences by software processes to reduce execution time

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: HERRINGTON K M; JEFFRIES K L
Number of Countries: 005 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 52713	A	19820602	EP 81107587	A	19810923	198223	B
CA 1162312	A	19840214				198412	
EP 52713	B	19880427				198817	
DE 3176724	G	19880601				198823	

Priority Applications (No Type Date): US 80208621 A 19801120
Cited Patents: 3.Jnl.Ref; No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 52713	A	E	28		
Designated States (Regional): DE FR GB IT					
EP 52713	B	E			
Designated States (Regional): DE FR GB IT					

Abstract (Basic): EP 52713 A

The processor memory stores processes each consisting of a control block, driver and drive program, each process having assigned to it a unique identity. Process management includes service and supervision routines for initialising the processes and for terminating them, for controlling their execution and for synchronising execution of two or more processes. One or more **queues** of work **requests** is associated with each process to schedule the work requests assigned to the processes. A priority coded interrupt signal is generated in response to processor input/output devices and to the processes.

In response to the priority coded interrupt signal a work **request** is assigned to a selected **queue** associated with the process to execute one of a predetermined subset of instructions stored in the memory. The highest priority process **driver** processes the highest priority work **request** of the highest priority **queue** by invoking one of the subset of **instructions** called by that work request. The completion of a given subset of instructions for a selected work request is signalled. Consequently, work requests are scheduled on an event or time interval basis.

47/5/11 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2005 JPO & JAPIO. All rts. reserv.

01477149 **Image available**
SYSTEM FOR CONTROLLING DATA TRANSFER

PUB. NO.: 59-188749 [JP 59188749 A]
PUBLISHED: October 26, 1984 (19841026)
INVENTOR(s): SUZUKI HIROSHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-062948 [JP 8362948]
FILED: April 12, 1983 (19830412)
INTL CLASS: [3] G06F-009/46; G06F-003/00; G06F-013/00
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic **Sequence** Units); 45.2 (**INFORMATION** PROCESSING -- Memory Units
JOURNAL: Section: P, Section No. 339, Vol. 09, No. 50, Pg. 67, March 05, 1985 (19850305)

ABSTRACT
PURPOSE: To always **arrange** transfer **requests** in the **order** of priority on a transfer request **queue** by giving the priority of the transfer request to a data transfer controlling routine.
CONSTITUTION: An acceptance routine 1 does not make direct registration of a transfer request in a transfer request queue QUE2, but fetches the priority of data transfer from priority information 15 in addition to parameters necessary to the data transfer given from a task 10 and gives the priority to a QUE rearrangement routine 5 together with the said parameters. The QUE rearrangement routine 5 compares the given priority with a transfer request priority stored on the QUE2 and rearranges the transfer requests on the QUE2

47/5/16 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2005 Thomson Derwent. All rts. reserv.

015522292 **Image available**
WPI Acc No: 2003-584439/200355
XRPX Acc No: N03-465154
Dynamic Random Access Memory accessing method in graphics processing system, involves grouping memory reads together in read group and memory writes together in write group **before executing memory** requests
Patent Assignee: ATI TECHNOLOGIES INC (ATIT-N)
Inventor: TANG M K; VAN HOOK T J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6564304	B1	20030513	US 2000653763	A	20000901	200355	B

Priority Applications (No Type Date): US 2000653763 A 20000901
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6564304	B1		10	G06F-013/14	

Abstract (Basic): US 6564304 B1
NOVELTY - The memory requests generated from the requesting masters, are stored in associated memory **request queues** . A **sort queue** (101) is connected to the request **queues** for receiving the requests and reordering the requests. The reordering step comprises grouping the memory reads together in a read group and memory writes together in write **group** before executing the memory **requests** .
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for graphics processing system.
USE - For accessing Dynamic RAM (DRAM) in graphics processing system (claimed). Also, applicable to double date rate synchronous dynamic RAM (DDR SDRAM).

ADVANTAGE - Minimizes read and write mode switching, thereby improving overall memory access performance.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of a DRAM system.

sort queue (101)

pp; 10 DwgNo 1/5

Title Terms: DYNAMIC; RANDOM; ACCESS; MEMORY; ACCESS; METHOD; GRAPHIC; PROCESS; SYSTEM; GROUP; MEMORY; READ; READ; GROUP; MEMORY; WRITING; WRITING; GROUP; EXECUTE; MEMORY; REQUEST

Derwent Class: T01; U14

International Patent Class (Main): G06F-013/14

File Segment: EPI

47/5/17 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2005 Thomson Derwent. All rts. reserv.

010437651 **Image available**

WPI Acc No: 1995-338968/199544

XRPX Acc No: N95-254322

Bus configuration for memory in computer systems - has segmented memory associated with respective slave controllers connected to master controller for storing transaction requests in queue for processing on first-received-first-done basis

Patent Assignee: HEWLETT-PACKARD CO (HEWP)

Inventor: HOTCHKISS T R; WILLIAMS J B; WOOD J L

Number of Countries: 003 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2288256	A	19951011	GB 954794	A	19950309	199544	B
DE 19503022	A1	19951012	DE 1003022	A	19950131	199546	
JP 7281988	A	19951027	JP 9594368	A	19950328	199601	

Priority Applications (No Type Date): US 94224941 A 19940408

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2288256	A		44	G06F-012/02	
DE 19503022	A1		17	G06F-013/16	
JP 7281988	A		17	G06F-013/16	

Abstract (Basic): GB 2288256 A

The system include memory units (108L, 108R-114L, 114R), which are grouped into segments and respective slave controllers (106U, 106L) that are connected to a master memory controller (302) which is provided for each segment. The single master memory controller receives a memory transaction request and stores the **requests** in **order** of receipt in a master **queue** . A single transaction bus (124) connects both the master and slave controllers. Each slave controller has a slave **transaction queue** (216) in which the **ordered** sequence of **transaction requests** are stored in the same order as the master **queue** .

The slave controller decodes the transaction request w.r.t the transaction type and address on a first-received-first-done basis. The slave controller responsible for the memory segment for the transaction at the head of the queues retains sole control of various data, buses and signals until the transaction is complete. The memory transaction is completed by accessing the memory having the transaction address and transferring the data between the master memory controller and the memory, only when the transaction request is an earliest received **request** in the ordered **sequence** . The slave controller signals to advance both the master and all of the slave queues, whenever the requests are completed. A data multiplexer is provided for each memory segment.

USE/ADVANTAGE - Eliminates multiplexer for applications needing less memory requirements. Each slave memory controller is assigned unique identification number to avoid refresh of DRAM chips at same time and to prevent power-consuming power spikes. Staggered refreshing

is provided. Avoids overlapping of refreshing operation, providing small step loads instead of single large step load on power system.

Dwg.3/3

Title Terms: BUS; CONFIGURATION; MEMORY; COMPUTER; SYSTEM; SEGMENT; MEMORY; ASSOCIATE; RESPECTIVE; SLAVE; CONTROL; CONNECT; MASTER; CONTROL; STORAGE; TRANSACTION; REQUEST; QUEUE; PROCESS; FIRST; RECEIVE; FIRST; BASIS

Derwent Class: T01

International Patent Class (Main): G06F-012/02; G06F-013/16

File Segment: EPI

File 348:EUROPEAN PATENTS 1978-2005/Feb W03
(c) 2005 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20050217,UT=20050210
(c) 2005 WIPO/Univentio

Set	Items	Description
S1	258097	QUEUE? ? OR BUFFER? ?
S2	12776	TIMESTAMP? OR TIME()STAMP?
S3	19	S1(7N)CREAT???(7N)S2
S4	92	S1(7N)(BEGIN? OR BEGAN OR START?)(7N)S2
S5	28	S4 AND IC=G06F
S6	26	S5 NOT S3
S7	18	S6 AND AC=US/PR
S8	17	S7 AND AY=(1970:2001)/PR
S9	20	S6 AND PY=1970:2001
S10	25	S8:S9
S11	1494	S1(5N)CREATED
S12	52	TIME(5N)S11
S13	1048	S1(5W)CREATED
S14	18	TIME(5W)S1(5W)CREATED

3/3,K/14 (Item 10 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2005 WIPO/Univentio. All rts. reserv.

00809830 **Image available**
SMART ELECTRONIC RECEIPT SYSTEM
SYSTEME DE FACTURES ELECTRONIQUES INTELLIGENTES
Patent Applicant/Assignee:
BRODIA, Suite 1530, 221 Main Street, San Francisco, CA 94105, US, US (Residence), US (Nationality)
Inventor(s):
HERMAN Gary, 1040 Dolores Street #307, San Francisco, CA 94110, US,
GOLDSTEIN Theodore C, 875 La Para Avenue, Palo Alto, CA 94306, US,
MARTINEZ Ronald G, 226 Francisco Street, San Francisco, CA 94133, US,
Legal Representative:
GLENN Michael A (et al) (agent), Glenn Patent Group, Suite L, 3475 Edison Way, Menlo Park, CA 94025, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200141527 A2-A3 20010614 (WO 0141527)
Application: WO 2000US20944 20000731 (PCT/WO US0020944)
Priority Application: US 99467545 19991210
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 26165

Fulltext Availability:
Detailed Description

Detailed Description
... that a log-switch failed.

This switch is accomplished as follows.

0) a memory-based **queue** is **created** to hold log-entries received during
5 the switch. Entries are **time - stamped** with their entry-time into the **queue** .

1) a new file is **created** under a temporary name. It will be automatically renamed after a successful log-switch has...

3/3,K/15 (Item 11 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2005 WIPO/Univentio. All rts. reserv.

00786021
SYSTEM AND METHOD FOR THE SYNCHRONIZATION AND DISTRIBUTION OF TELEPHONY TIMING INFORMATION IN A CABLE MODEM NETWORK
SYSTEME ET PROCEDE DESTINE A LA SYNCHRONISATION ET A LA DISTRIBUTION D'INFORMATIONS DE SYNCHRONISATION TELEPHONIQUES SUR UN RESEAU MODEM CABLE
Patent Applicant/Assignee:
BROADCOM CORPORATION, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
RABENKO Theodore F, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US

(Residence), US (Nationality), (Designated only for: US)
DENNEY Lisa V, 16215 Alton Parkway, Irvine, CA 92618-3616, US, US
(Residence), US (Nationality), (Designated only for: US)
Legal Representative:
GELFOUND Craig A (agent), Christie, Parker & Hale, LLP, P.O. Box 7068, Pasadena, CA 91109-7068, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200119005 A1 20010315 (WO 0119005)
Application: WO 2000US24405 20000905 (PCT/WO US0024405)
Priority Application: US 99152254 19990903
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE
ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT
LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM
TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 112078

Fulltext Availability:
Detailed Description

Detailed Description
... the length of the data on the block, and/or asserted first and or last **buffer** flags.
The described exemplary network gateway can include a voice processor 160 for processing and...

3/3,K/16 (Item 12 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2005 WIPO/Univentio. All rts. reserv.

00766332 **Image available**
SYSTEM AND METHOD FOR RECEIVING OVER A NETWORK A BROADCAST FROM A BROADCAST SOURCE
SYSTEME ET PROCEDE DE RECEPTION D'UNE EMISSION SUR RESEAU A PARTIR D'UNE STATION DE RADIODIFFUSION
Patent Applicant/Assignee:
THE TRUSTEES OF COLUMBIA UNIVERSITY IN THE CITY OF NEW YORK, 116th Street and Broadway, New York, NY 10027, US, US (Residence), US (Nationality)
Inventor(s):
DUTTA Ashutosh, 560 Riverside Drive, Apt. 17C, New York, NY 10027, US
SCHULZRINNE Henning, 313 Westview Avenue, Leonia, NJ 07605, US
YEMINI Yechiam, 223 Promenade, Edgewater, NJ 07020, US
Legal Representative:
TANG Henry, Baker Botts LLP, 30 Rockefeller Plaza, New York, NY 10112-0228, US
Patent and Priority Information (Country, Number, Date):
Patent: WO 200079734 A1 20001228 (WO 0079734)
Application: WO 2000US16913 20000619 (PCT/WO US0016913)
Priority Application: US 99139933 19990618
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE
ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT
LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM
TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW

(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 49708

Fulltext Availability:
Claims

Claim
... the privacy header field) .
public byte[] payload @ null;
The date and time cf the packet **created** .
public long **timeStamp** = -1;
The maximum payload **buffer** length (currently IK byte3 a3 limited by SAP).
public final static int MAX.BUFLEN = 1024...

3/3,K/17 (Item 13 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2005 WIPO/Univentio. All rts. reserv.

00504433 **Image available**
TRANSMITTING REVISIONS WITH DIGITAL SIGNATURES
TRANSMISSION DE REVISIONS COMPORTANT DES SIGNATURES NUMERIQUES
Patent Applicant/Assignee:
KONINKLIJKE PHILIPS ELECTRONICS N V,
PHILIPS AB,
Inventor(s):
EPSTEIN Michael,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9935785 A2 19990715
Application: WO 98IB2120 19981228 (PCT/WO IB9802120)
Priority Application: US 972098 19971231
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
CA CN JP KR AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 9050

Fulltext Availability:
Detailed Description

Detailed Description
... buffer 471 onto the network. Program module 472 reads the server's signature from the **buffer** and **creates** a **time stamp** containing: the server's signature, the time that the server's signature was received (in...

3/3,K/18 (Item 14 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2005 WIPO/Univentio. All rts. reserv.

00456627 **Image available**
VIRTUAL PROPERTY SYSTEM
BIENS VIRTUELS EN RESEAU
Patent Applicant/Assignee:
TRANSACTOR NETWORKS INC,
Inventor(s):
MARTINEZ Ronald,
SCHNEIER Bruce,
GUERIN Greg,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9847091 A1 19981022
Application: WO 98US7176 19980409 (PCT/WO US9807176)
Priority Application: US 97834027 19970411

Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM
GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX
NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW GH GM
KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI
FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 21246

Fulltext Availability:
Detailed Description

Detailed Description
... that a log-switch failed. This switch is accomplished as follows.

0) a memory-based **queue** is **created** to hold log-entries received during the I 0 switch. Entries are **time - stamped** with their entry-time into the **queue** .

I) a new file is **created** under a temporary name. It will be automatically renamed after a successfbl log-switch has...

3/3,K/19 (Item 15 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2005 WIPO/Univentio. All rts. reserv.

00300264 **Image available**
QUEUE MANAGEMENT IN A DATA PROCESSING LINK
GESTION D'UNE FILE D'ATTENTE DANS UN SYSTEME DE TRAITEMENT DE DONNEES
Patent Applicant/Assignee:
INTERNATIONAL BUSINESS MACHINES CORPORATION,
BANKS Timothy William,
WEEDEN Paul,
TURNER Kevin John,
WYATT David John,
Inventor(s):
BANKS Timothy William,
WEEDEN Paul,
TURNER Kevin John,
WYATT David John,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9518415 A1 19950706
Application: WO 93GB2673 19931230 (PCT/WO GB9302673)
Priority Application: WO 93GB2673 19931230
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
JP US AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 5409

Fulltext Availability:
Detailed Description

Detailed Description
... the allocator 110 creates and
stores the following additional parameters for use in managing the **queue**

130. Each request for a link has its own set of these parameters.

AQTS **Time stamp** indicating the time tile **queue** 130 of requests was started (this is **created** by step 205 in Fig. 2)
ACNT The number of requests processed since the queue...